

[illegible][illegible][illegible][illegible]

AM2-->AM3 Different: AE9-->AE7,  
H22-->H20. Extra pin: B2 AM3 socket is  
938 pins. Only shift 2 pins.

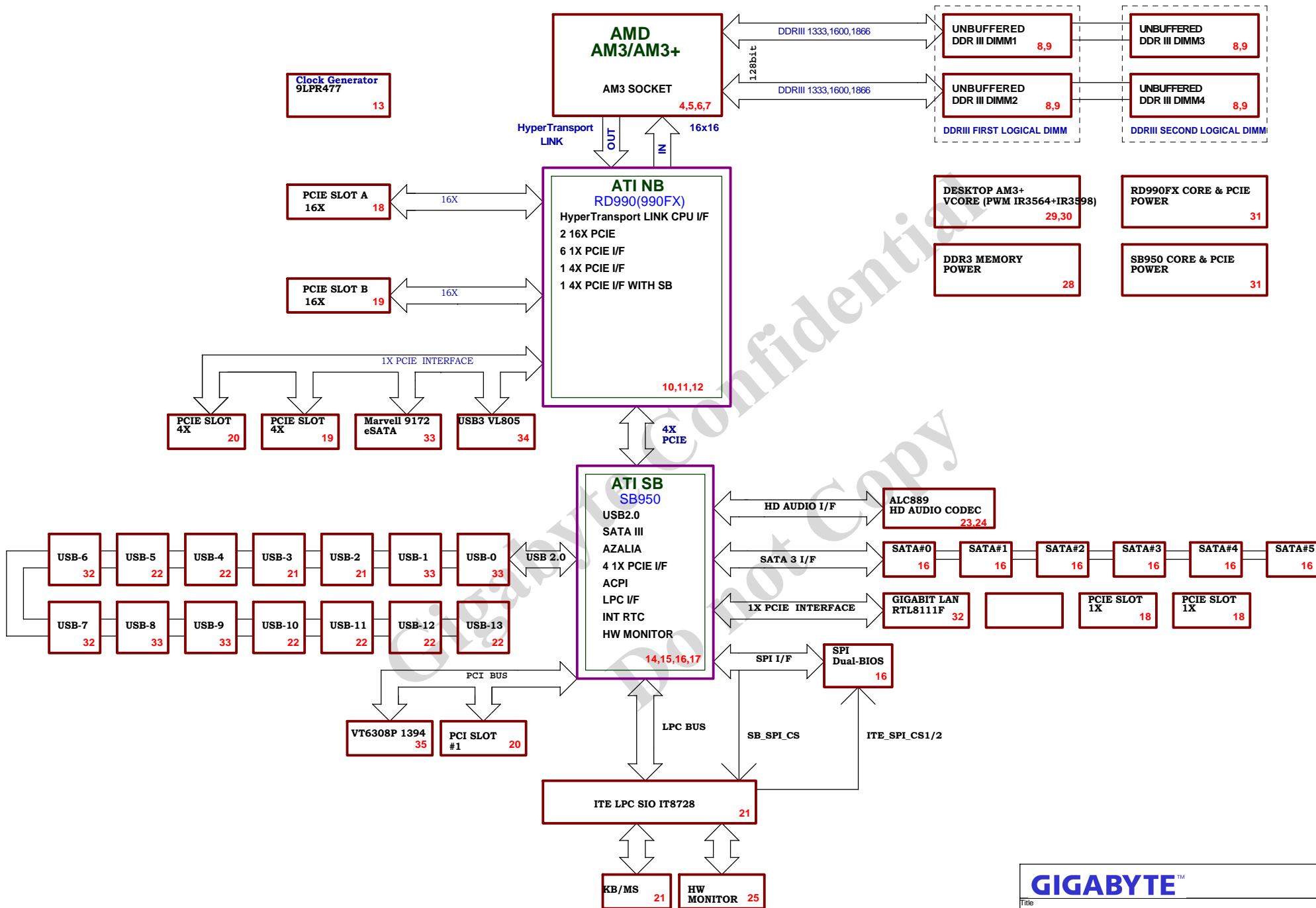
4 Layer, 4mil 50ohm +/- 15% X

**P-Code:**  
**U98145-0**

### Circuit or PCB layout change for next version

GIGABYTE™

Size Custom	Document Number <b>GA-990FXA-UD3</b>	Rev <b>4.01</b>
Date:	Wednesday, July 17, 2013	Sheet 2 of 35

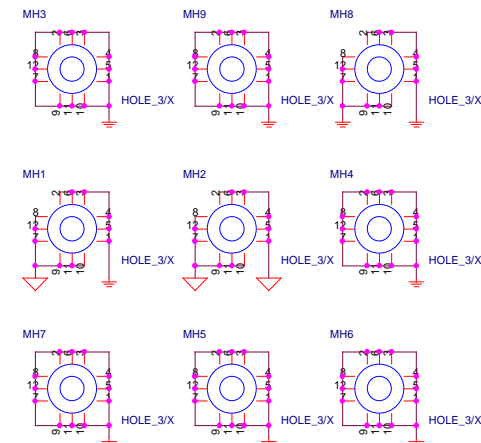
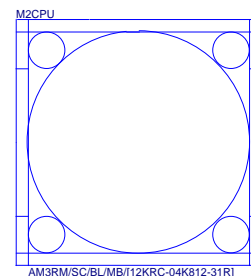
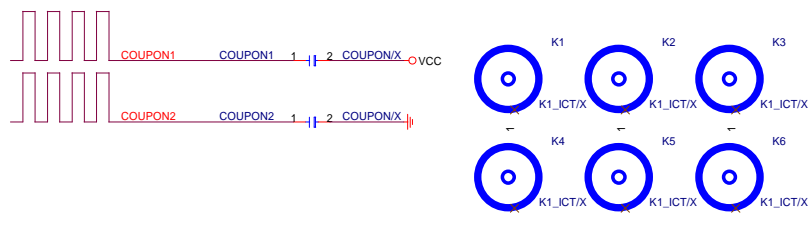
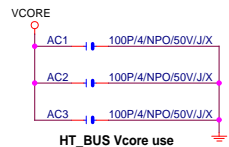


**GIGABYTE™**

Title			
BLOCK DIAGRAM			
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	4.01	
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```
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12
```

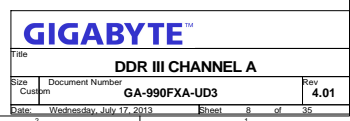
```
VLDT_A = VCC12_HT
VLDT_B = HT12B
```

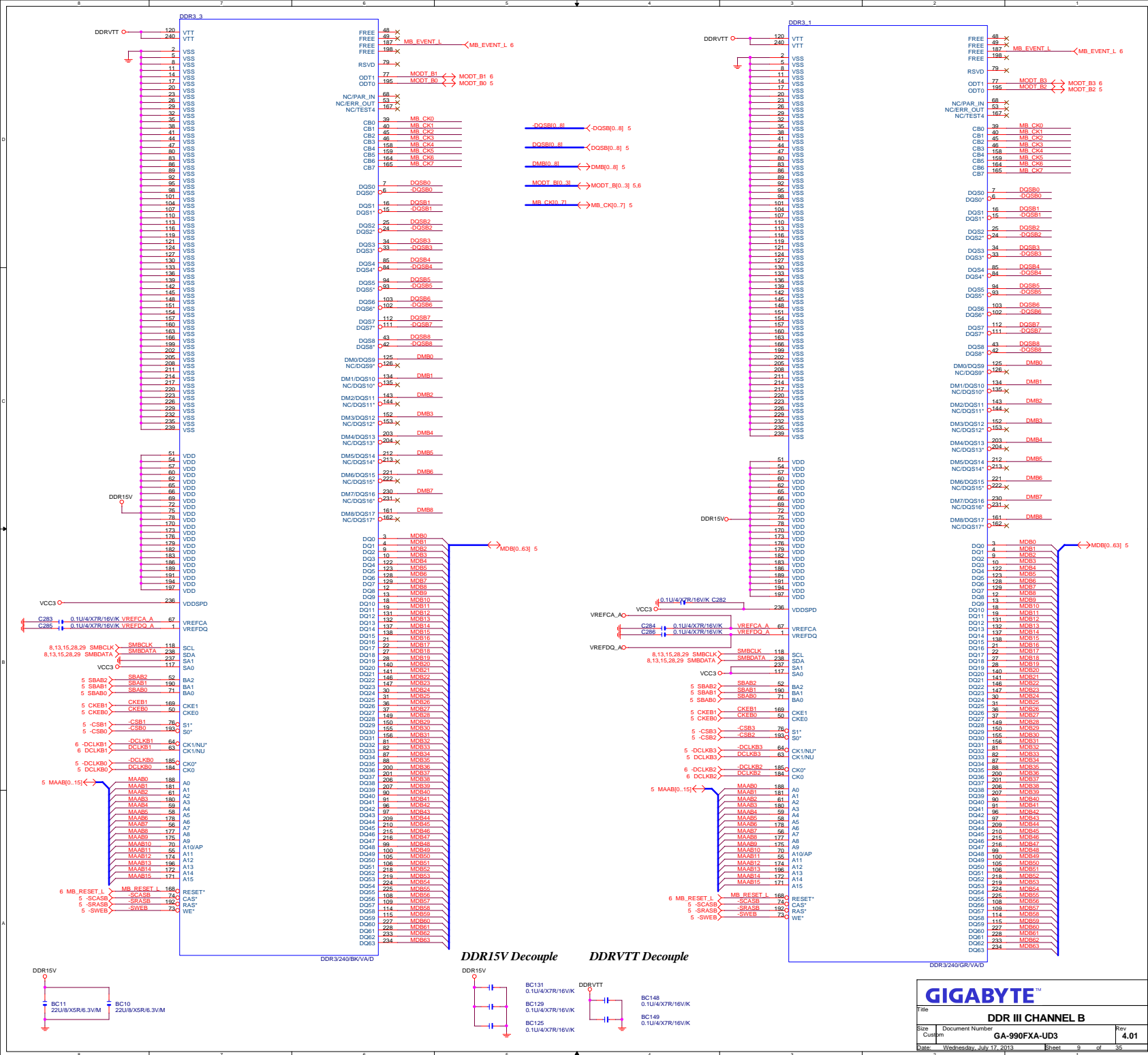






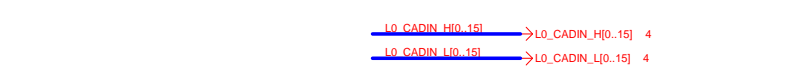






U3A				PART 1/5			
L0_CADOUT_H15	T25	HT_RXCAD15P	HT_TXCAD15P	N23	L0_CADIN_H15		
L0_CADOUT_L15	T24	HT_RXCAD15N	HT_TXCAD15N	N24	L0_CADIN_L15		
L0_CADOUT_H14	U24	HT_RXCAD14P	HT_TXCAD14P	M25	L0_CADIN_H14		
L0_CADOUT_L14	U23	HT_RXCAD14N	HT_TXCAD14N	M24	L0_CADIN_L14		
L0_CADOUT_H13	V25	HT_RXCAD13P	HT_TXCAD13P	L23	L0_CADIN_H13		
L0_CADOUT_L13	V24	HT_RXCAD13N	HT_TXCAD13N	L24	L0_CADIN_L13		
L0_CADOUT_H12	W24	HT_RXCAD12P	HT_TXCAD12P	K24	L0_CADIN_H12		
L0_CADOUT_L12	W23	HT_RXCAD12N	HT_TXCAD12N	K25	L0_CADIN_L12		
L0_CADOUT_H11	AA24	HT_RXCAD11P	HT_TXCAD11P	H24	L0_CADIN_H11		
L0_CADOUT_L11	AA23	HT_RXCAD11N	HT_TXCAD11N	H25	L0_CADIN_L11		
L0_CADOUT_H10	AB25	HT_RXCAD10P	HT_TXCAD10P	G23	L0_CADIN_H10		
L0_CADOUT_L10	AB24	HT_RXCAD10N	HT_TXCAD10N	G24	L0_CADIN_L10		
L0_CADOUT_H9	AC24	HT_RXCAD9P	HT_TXCAD9P	E24	L0_CADIN_H9		
L0_CADOUT_L9	AC23	HT_RXCAD9N	HT_TXCAD9N	F25	L0_CADIN_L9		
L0_CADOUT_H8	AD25	HT_RXCAD8P	HT_TXCAD8P	E23	L0_CADIN_H8		
L0_CADOUT_L8	AD24	HT_RXCAD8N	HT_TXCAD8N	E24	L0_CADIN_L8		
L0_CADOUT_H7	T28	HT_RXCAD7P	HT_TXCAD7P	N26	L0_CADIN_H7		
L0_CADOUT_L7	T27	HT_RXCAD7N	HT_TXCAD7N	M27	L0_CADIN_L7		
L0_CADOUT_H6	U27	HT_RXCAD6P	HT_TXCAD6P	M28	L0_CADIN_H6		
L0_CADOUT_L6	U26	HT_RXCAD6N	HT_TXCAD6N	L26	L0_CADIN_L6		
L0_CADOUT_H5	V28	HT_RXCAD5P	HT_TXCAD5P	L27	L0_CADIN_H5		
L0_CADOUT_L5	V27	HT_RXCAD5N	HT_TXCAD5N	K27	L0_CADIN_L5		
L0_CADOUT_H4	W27	HT_RXCAD4P	HT_TXCAD4P	K28	L0_CADIN_L4		
L0_CADOUT_L4	W26	HT_RXCAD4N	HT_TXCAD4N	J28	L0_CADIN_L3		
L0_CADOUT_H3	AA27	HT_RXCAD3P	HT_TXCAD3P	G26	L0_CADIN_H2		
L0_CADOUT_L3	AA26	HT_RXCAD3N	HT_TXCAD3N	G27	L0_CADIN_L2		
L0_CADOUT_H2	AB28	HT_RXCAD2P	HT_TXCAD2P	F28	L0_CADIN_H1		
L0_CADOUT_L2	AB27	HT_RXCAD2N	HT_TXCAD2N	E28	L0_CADIN_L1		
L0_CADOUT_H1	AC27	HT_RXCAD1P	HT_TXCAD1P	E26	L0_CADIN_H0		
L0_CADOUT_L1	AC26	HT_RXCAD1N	HT_TXCAD1N	E27	L0_CADIN_L0		
L0_CADOUT_H0	AD28	HT_RXCAD0P	HT_TXCAD0P				
L0_CADOUT_L0	AD27	HT_RXCAD0N	HT_TXCAD0N				

4 L0_CLKOUT_H1	L0_CLKOUT_H1	Y25	HT_RXCLK1P	HT_TXCLK1P	J23	L0_CLKIN_H1	L0_CLKIN_H1	4
4 L0_CLKOUT_L1	L0_CLKOUT_L1	Y24	HT_RXCLK1N	HT_TXCLK1N	J24	L0_CLKIN_L1	L0_CLKIN_L1	4
4 L0_CLKOUT_H0	L0_CLKOUT_H0	Y28	HT_RXCLK0P	HT_TXCLK0P	J26	L0_CLKIN_H0	L0_CLKIN_H0	4
4 L0_CLKOUT_L0	L0_CLKOUT_L0	Y27	HT_RXCLK0N	HT_TXCLK0N	J27	L0_CLKIN_L0	L0_CLKIN_L0	4
4 L0_CTOUT_H1	L0_CTOUT_H1	R24	HT_RXCTL1P	HT_TXCTL1P	P24	L0_CTIN_H1	L0_CTIN_H1	4
4 L0_CTOUT_L1	L0_CTOUT_L1	R23	HT_RXCTL1N	HT_TXCTL1N	P25	L0_CTIN_L1	L0_CTIN_L1	4
4 L0_CTOUT_H0	L0_CTOUT_H0	R27	HT_RXCTL0P	HT_TXCTL0P	P28	L0_CTIN_H0	L0_CTIN_H0	4
4 L0_CTOUT_L0	L0_CTOUT_L0	R26	HT_RXCTL0N	HT_TXCTL0N	P27	L0_CTIN_L0	L0_CTIN_L0	4



4 L0_CADOUT_H10_15	L0_CADOUT_H10_15							
4 L0_CADOUT_L10_15	L0_CADOUT_L10_15							
EXP_A_RXP10_15	EXP_A_RXP10_15	18						
EXP_A_RXN10_15	EXP_A_RXN10_15	18						
EXP_A_TXP10_15	EXP_A_TXP10_15	18						
EXP_A_TXN10_15	EXP_A_TXN10_15	18						
EXP_B_TXP10_15	EXP_B_TXP10_15	19						
EXP_B_TXN10_15	EXP_B_TXN10_15	19						
EXP_B_RXP10_15	EXP_B_RXP10_15	19						
EXP_B_RXN10_15	EXP_B_RXN10_15	19						

EXP_B_TXP10_15	EXP_B_TXP10_15	19						
EXP_B_TXN10_15	EXP_B_TXN10_15	19						
EXP_B_RXP10_15	EXP_B_RXP10_15	19						
EXP_B_RXN10_15	EXP_B_RXN10_15	19						
20 PCIE4_4P	AD11	GPP3_RX9P	AD11	GPP3_RX9P	AD11	GPP3_RX9P	AD11	GPP3_RX9P
20 PCIE4_4N	AD11	GPP3_RX9N	AD11	GPP3_RX9N	AD11	GPP3_RX9N	AD11	GPP3_RX9N
20 PCIE4_3P	AD12	GPP3_RX8P	AD12	GPP3_RX8P	AD12	GPP3_RX8P	AD12	GPP3_RX8P
20 PCIE4_3N	AD12	GPP3_RX8N	AD12	GPP3_RX8N	AD12	GPP3_RX8N	AD12	GPP3_RX8N
20 PCIE4_2P	AD13	GPP3_RX7P	AD13	GPP3_RX7P	AD13	GPP3_RX7P	AD13	GPP3_RX7P
20 PCIE4_2N	AD13	GPP3_RX7N	AD13	GPP3_RX7N	AD13	GPP3_RX7N	AD13	GPP3_RX7N
20 PCIE4_1P	AD14	GPP3_RX6P	AD14	GPP3_RX6P	AD14	GPP3_RX6P	AD14	GPP3_RX6P
20 PCIE4_1N	AD14	GPP3_RX6N	AD14	GPP3_RX6N	AD14	GPP3_RX6N	AD14	GPP3_RX6N
33 RB_SL_IN	AD15	GPP3_RX5P	AD15	GPP3_RX5P	AD15	GPP3_RX5P	AD15	GPP3_RX5P
34 UB_USB3_IN	AD16	GPP3_RX4P	AD16	GPP3_RX4P	AD16	GPP3_RX4P	AD16	GPP3_RX4P
34 UB_USB3_N	AD16	GPP3_RX4N	AD16	GPP3_RX4N	AD16	GPP3_RX4N	AD16	GPP3_RX4N
19 PCIE4_4P_SB	AD17	GPP3_RX3P	AD17	GPP3_RX3P	AD17	GPP3_RX3P	AD17	GPP3_RX3P
19 PCIE4_4N_SB	AD17	GPP3_RX3N	AD17	GPP3_RX3N	AD17	GPP3_RX3N	AD17	GPP3_RX3N
19 PCIE4_3P_SB	AD18	GPP3_RX2P	AD18	GPP3_RX2P	AD18	GPP3_RX2P	AD18	GPP3_RX2P
19 PCIE4_2P_SB	AD18	GPP3_RX2N	AD18	GPP3_RX2N	AD18	GPP3_RX2N	AD18	GPP3_RX2N
19 PCIE4_2N_SB	AD19	GPP3_RX1P	AD19	GPP3_RX1P	AD19	GPP3_RX1P	AD19	GPP3_RX1P
19 PCIE4_1P_SB	AD19	GPP3_RX1N	AD19	GPP3_RX1N	AD19	GPP3_RX1N	AD19	GPP3_RX1N
19 PCIE4_1N_SB	AD20	GPP3_RX0P	AD20	GPP3_RX0P	AD20	GPP3_RX0P	AD20	GPP3_RX0P



U3B				PART 2/5			
EXP_A_RXP15	N6	GPP1_RX15P	GPP1_RX15P	N3	EXP_A_TXP15		
EXP_A_RXN15	N5	GPP1_RX15N	GPP1_RX15N	N2	EXP_A_TXN15		
EXP_A_RXP14	M5	GPP1_RX14P	GPP1_RX14P	M2	EXP_A_TXP14		
EXP_A_RXN14	M4	GPP1_RX14N	GPP1_RX14N	M1	EXP_A_TXN14		
EXP_A_RXP13	L5	GPP1_RX13P	GPP1_RX13P	L3	EXP_A_TXP13		
EXP_A_RXN13	L4	GPP1_RX13N	GPP1_RX13N	L2	EXP_A_TXN13		
EXP_A_RXP12	K5	GPP1_RX12P	GPP1_RX12P	K2	EXP_A_TXP12		
EXP_A_RXN12	K4	GPP1_RX12N	GPP1_RX12N	K1	EXP_A_TXN12		
EXP_A_RXP11	J5	GPP1_RX11P	GPP1_RX11P	J3	EXP_A_TXP11		
EXP_A_RXN11	J4	GPP1_RX11N	GPP1_RX11N	J2	EXP_A_TXN11		
EXP_A_RXP10	H5	GPP1_RX10P	GPP1_RX10P	H2	EXP_A_TXP10		
EXP_A_RXN10	H4	GPP1_RX10N	GPP1_RX10N	H1	EXP_A_TXN10		
EXP_A_RXP9	G6	GPP1_RX9P	GPP1_RX9P	G3	EXP_A_TXP9		
EXP_A_RXN9	G5	GPP1_RX9N	GPP1_RX9N	G2	EXP_A_TXN9		
EXP_A_RXP8	F6	GPP1_RX8P	GPP1_RX8P	F2	EXP_A_TXP8		
EXP_A_RXN8	F5	GPP1_RX8N	GPP1_RX8N	F1	EXP_A_TXN8		
EXP_A_RXP7	D2	GPP1_RX7P	GPP1_RX7P	E3	EXP_A_TXP7		
EXP_A_RXN7	D1	GPP1_RX7N	GPP1_RX7N	E2	EXP_A_TXN7		
EXP_A_RXP6	B6	GPP1_RX6P	GPP1_RX6P	A4	EXP_A_TXP6		
EXP_A_RXN6	B5	GPP1_RX6N	GPP1_RX6N	B4	EXP_A_TXN6		
EXP_A_RXP5	C6	GPP1_RX5P	GPP1_RX5P	A6	EXP_A_TXP5		
EXP_A_RXN5	E6	GPP1_RX5N	GPP1_RX5N	B6	EXP_A_TXN5		
EXP_A_RXP4	E7	GPP1_RX4P	GPP1_RX4P	B7	EXP_A_TXP4		
EXP_A_RXN4	D7	GPP1_RX4N	GPP1_RX4N	C7	EXP_A_TXN4		
EXP_A_RXP3	E8	GPP1_RX3P	GPP1_RX3P	A8	EXP_A_TXP3		
EXP_A_RXN3	E9	GPP1_RX3N	GPP1_RX3N	B8	EXP_A_TXN3		
EXP_A_RXP2	F9	GPP1_RX2P	GPP1_RX2P	B9	EXP_A_TXP2		
EXP_A_RXN2	F8	GPP1_RX2N	GPP1_RX2N	C3	EXP_A_TXN2		
EXP_A_RXP1	D10	GPP1_RX1P	GPP1_RX1P	A10	EXP_A_TXP1		
EXP_A_RXN1	E10	GPP1_RX1N	GPP1_RX1N	B10	EXP_A_TXN1		
EXP_A_RXP0	E11	GPP1_RX0P	GPP1_RX0P	B11	EXP_A_TXP0		
EXP_A_RXN0	F11	GPP1_RX0N	GPP1_RX0N	C11	EXP_A_TXN0		

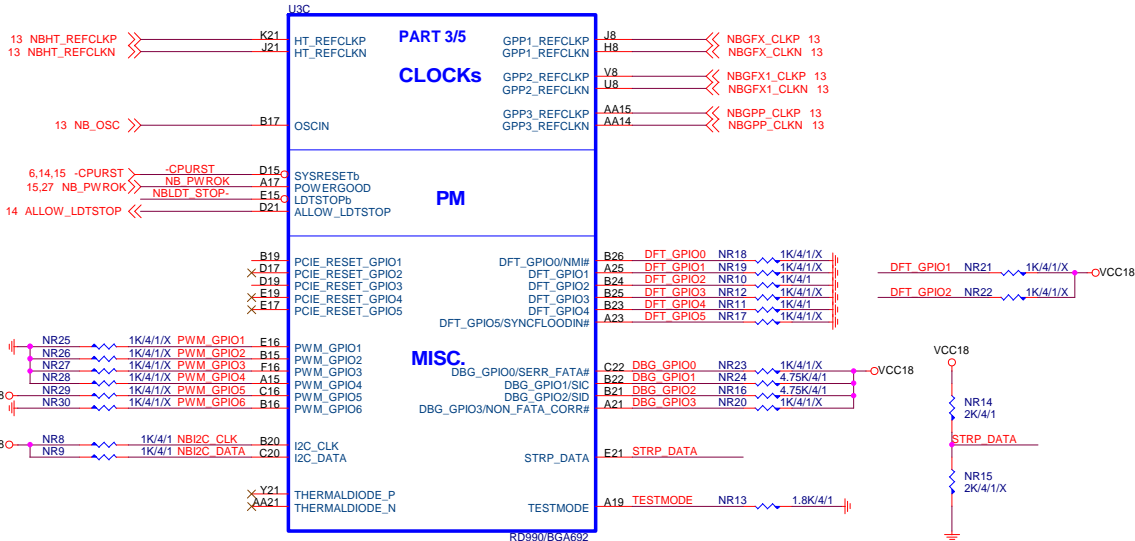
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EXP_B_RXN15	AD9	GPP2_RX15N	GPP2_RX15N	AG9	EXP_B_TXN15		
EXP_B_RXP14	AE9	GPP2_RX14P	GPP2_RX14P	AH9	EXP_B_TXP14		
EXP_B_RXN14	AE8	GPP2_RX14N	GPP2_RX14N	AF7	EXP_B_TXP13		
EXP_B_RXP13	AC7	GPP2_RX13P	GPP2_RX13P	AG7	EXP_B_TXP12		
EXP_B_RXN13	AD7	GPP2_RX13N	GPP2_RX13N	AH6	EXP_B_TXN12		
EXP_B_RXP12	AE6	GPP2_RX12P	GPP2_RX12P	AG4	EXP_B_TXP11		
EXP_B_RXN12	AE5	GPP2_RX12N	GPP2_RX12N	AH4	EXP_B_TXN11		
EXP_B_RXP11	AF5	GPP2_RX11P	GPP2_RX11P	AE3	EXP_B_TXP10		
EXP_B_RXN11	AG5	GPP2_RX11N	GPP2_RX11N	AE2	EXP_B_TXN10		
EXP_B_RXP10	AE2	GPP2_RX10P	GPP2_RX10P	AC3	EXP_B_TXP9		
EXP_B_RXN10	AD2	GPP2_RX10N	GPP2_RX10N	AC2	EXP_B_TXN9		
EXP_B_RXP9	AD1	GPP2_RX9P	GPP2_RX9P	AB2	EXP_B_TXP8		
EXP_B_RXN9	AB5	GPP2_RX9N	GPP2_RX9N	AB1	EXP_B_TXN8		
EXP_B_RXP8	AB4	GPP2_RX8P	GPP2_RX8P	AA3	EXP_B_TXP7		
EXP_B_RXN8	AA6	GPP2_RX8N	GPP2_RX8N	AA2	EXP_B_TXN7		
EXP_B_RXP7	AA5	GPP2_RX7P	GPP2_RX7P	Y2	EXP_B_TXP6		
EXP_B_RXN7	Y5	GPP2_RX7N	GPP2_RX7N	Y1	EXP_B_TXN6		
EXP_B_RXP6	Y4	GPP2_RX6P	GPP2_RX6P	W3	EXP_B_TXP5		
EXP_B_RXN6	W6	GPP2_RX6N	GPP2_RX6N	W2	EXP_B_TXN5		
EXP_B_RXP5	W5	GPP2_RX5P	GPP2_RX5P	V2	EXP_B_TXP4		
EXP_B_RXN5	V5	GPP2_RX5N	GPP2_RX5N	V1	EXP_B_TXN4		
EXP_B_RXP4	V4	GPP2_RX4P	GPP2_RX4P	U3	EXP_B_TXP3		
EXP_B_RXN4	U6	GPP2_RX4N	GPP2_RX4N	U2	EXP_B_TXN3		
EXP_B_RXP3	U5	GPP2_RX3P	GPP2_RX3P	T2	EXP_B_TXP2		
EXP_B_RXN3	U5	GPP2_RX3N	GPP2_RX3N	T1	EXP_B_TXN2		
EXP_B_RXP2	T5	GPP2_RX2P	GPP2_RX2P	R3	EXP_B_TXP1		
EXP_B_RXN2	T4	GPP2_RX2N	GPP2_RX2N	R2	EXP_B_TXN1		
EXP_B_RXP1	R6	GPP2_RX1P	GPP2_RX1P	P2	EXP_B_TXP0		
EXP_B_RXN1	R6	GPP2_RX1N	GPP2_RX1N	P1	EXP_B_TXN0		
EXP_B_RXP0	P4	GPP2_RX0P	GPP2_RX0P				
EXP_B_RXN0	P4	GPP2_RX0N	GPP2_RX0N				

20 PCIE4_4P	AD11	GPP3_RX9P	AD11	GPP3_RX9P	AD11	GPP3_RX9P	AD11	GPP3_RX9P
20 PCIE4_4N	AD11	GPP3_RX9N	AD11	GPP3_RX9N	AD11	GPP3_RX9N	AD11	GPP3_RX9N
20 PCIE4_3P	AD12	GPP3_RX8P	AD12	GPP3_RX8P	AD12	GPP3_RX8P	AD12	GPP3_RX8P
20 PCIE4_3N	AD12	GPP3_RX8N	AD12	GPP3_RX8N	AD12	GPP3_RX8N	AD12	GPP3_RX8N
20 PCIE4_2P	AD13	GPP3_RX7P	AD13	GPP3_RX7P	AD13	GPP3_RX7P	AD13	GPP3_RX7P
20 PCIE4_2N	AD13	GPP3_RX7N	AD13	GPP3_RX7N	AD13	GPP3_RX7N	AD13	GPP3_RX7N
20 PCIE4_1P	AD14	GPP3_RX6P	AD14	GPP3_RX6P	AD14	GPP3_RX6P	AD14	GPP3_RX6P
20 PCIE4_1N	AD14	GPP3_RX6N	AD14	GPP3_RX6N	AD14	GPP3_RX6N	AD14	GPP3_RX6N
33 RB_SL_IN	AD15	GPP3_RX5P	AD15	GPP3_RX5P	AD15	GPP3_RX5P	AD15	GPP3_RX5P
34 UB_USB3_IN	AD16	GPP3_RX4P	AD16	GPP3_RX4P	AD16	GPP3_RX4P	AD16	GPP3_RX4P
34 UB_USB3_N	AD16	GPP3_RX4N	AD16	GPP3_RX4N	AD16	GPP3_RX4N	AD16	GPP3_RX4N
19 PCIE4_4P_SB	AD17	GPP3_RX3P	AD17	GPP3_RX3P	AD17	GPP3_RX3P	AD17	GPP3_RX3P
19 PCIE4_4N_SB	AD17	GPP3_RX3N	AD17	GPP3_RX3N	AD17	GPP3_RX3N	AD17	GPP3_RX3N
19 PCIE4_3P_SB	AD18	GPP3_RX2P	AD18	GPP3_RX2P	AD18	GPP3_RX2P	AD18	GPP3_RX2P
19 PCIE4_2P_SB	AD18	GPP3_RX2N	AD18	GPP3_RX2N	AD18	GPP3_RX2N	AD18	GPP3_RX2N
19 PCIE4_2N_SB	AD19	GPP3_RX1P	AD19	GPP3_RX1P	AD19	GPP3_RX1P	AD19	GPP3_RX1P
19 PCIE4_1P_SB	AD19	GPP3_RX1N	AD19	GPP3_RX1N	AD19	GPP3_RX1N	AD19	GPP3_RX1N
19 PCIE4_1N_SB	AD20	GPP3_RX0P	AD20	GPP3_RX0P	AD20	GPP3_RX0P	AD20	GPP3_RX0P

14 A_RX3P	AC21	SB_RX3P
14 A_RX3N	AD21	SB_RX3N
14 A_RX2P	AD22	SB_RX2P
14 A_RX2N	AE22	SB_RX2N
14 A_RX1P	AF25	SB_RX1P
14 A_RX1N	AG25	SB_RX1N
14 A_RX0P	AG26	SB_RX0P
14 A_RX0N	AH26	SB_RX0N

NB_VCC	NR2	1.27K/4/1	AE20	PCE_BCALRP
	NR3	1.82K/4/1	AD20	PCE_BCALRN
	NR4	1.27K/4/1	AE10	PCE_RCALRP
	NR5	1.82K/4/1	AD10	PCE_RCALRN
	NR6	1.27K/4/1	F14	PCE_TCALRP
	NR7	1.82K/4/1	E14	PCE_TCALRN



#### DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb

Enables the Test Debug Bus using GPIO.  
1 : Disable ( Can still be enabled using nbcfg register access)  
0 : Enable

#### DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

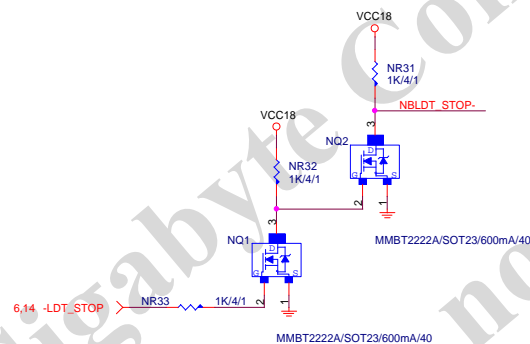
These pin straps are used to configure PCI-E GPP mode.  
GPIO4:3:2  
000 : 4:2:4 B  
001 : 4:1:1:4 C  
010 : 1:1:1:1:1:1:4 L (Hardware Default)  
011 : 2:1:1:1:1:1:4 E  
100 : 2:2:1:1:4 K  
101 : 2:2:2:4 C2  
110 : Hardware default (mode L) or EEPROM  
111 : Hardware default (mode L) or EEPROM  
101 : 01100  
111 : 01011

#### DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

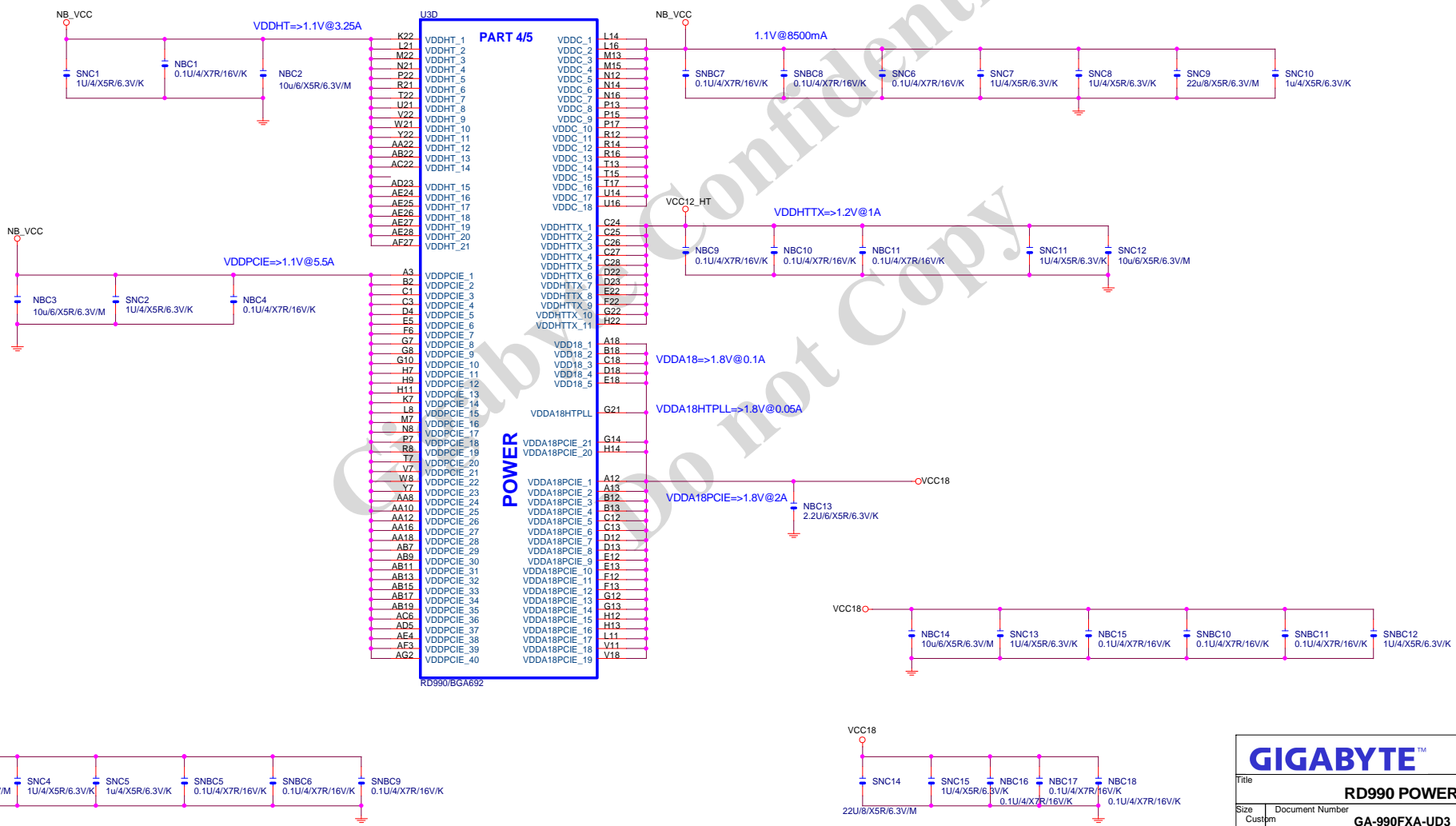
#### DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb

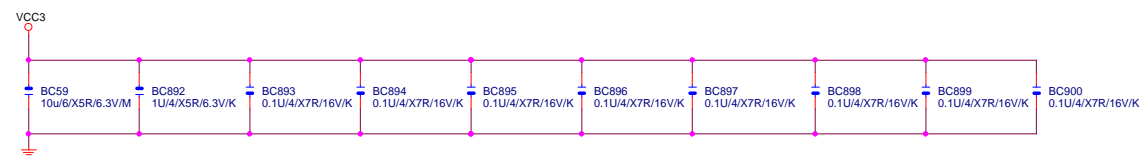
Enables the Test Debug Bus using PCIE bus  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable



**GIGABYTE**™

Title		RD990 CLOCK & SYSB I/F	
Size	Document Number	GA-990FXA-UD3	Rev
Custom			4.01
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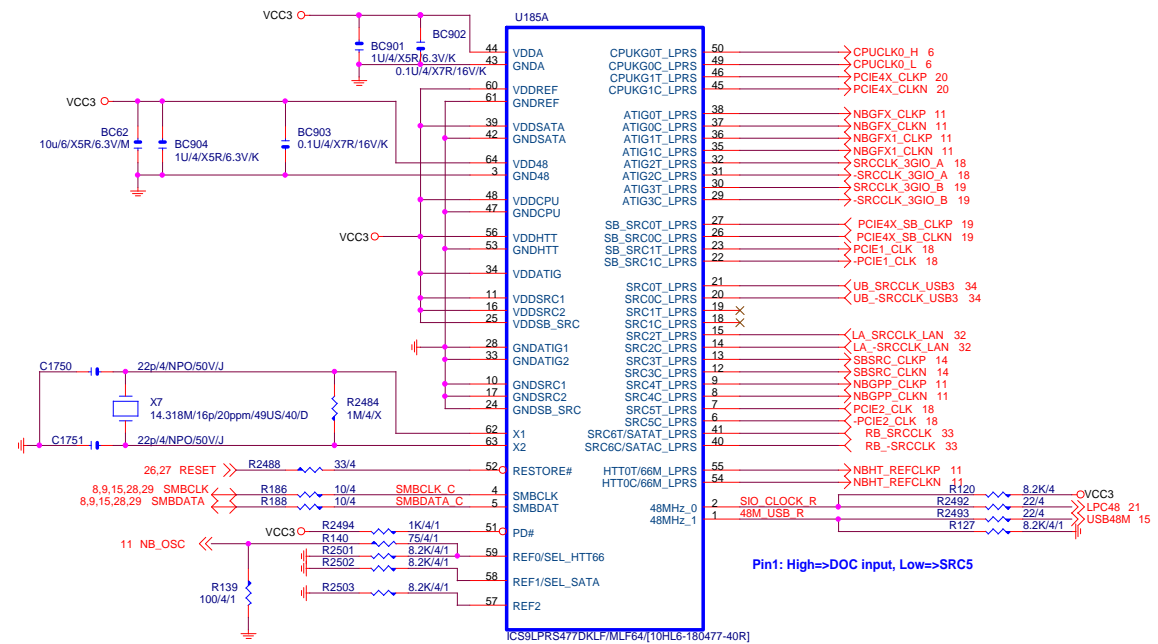




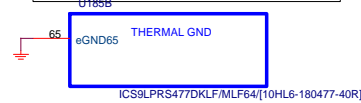
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* the GFX\_REFCLK input is required for all cases



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

**GIGABYTE™**

TitleICS9LPRS477

SizeCustom

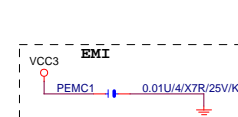
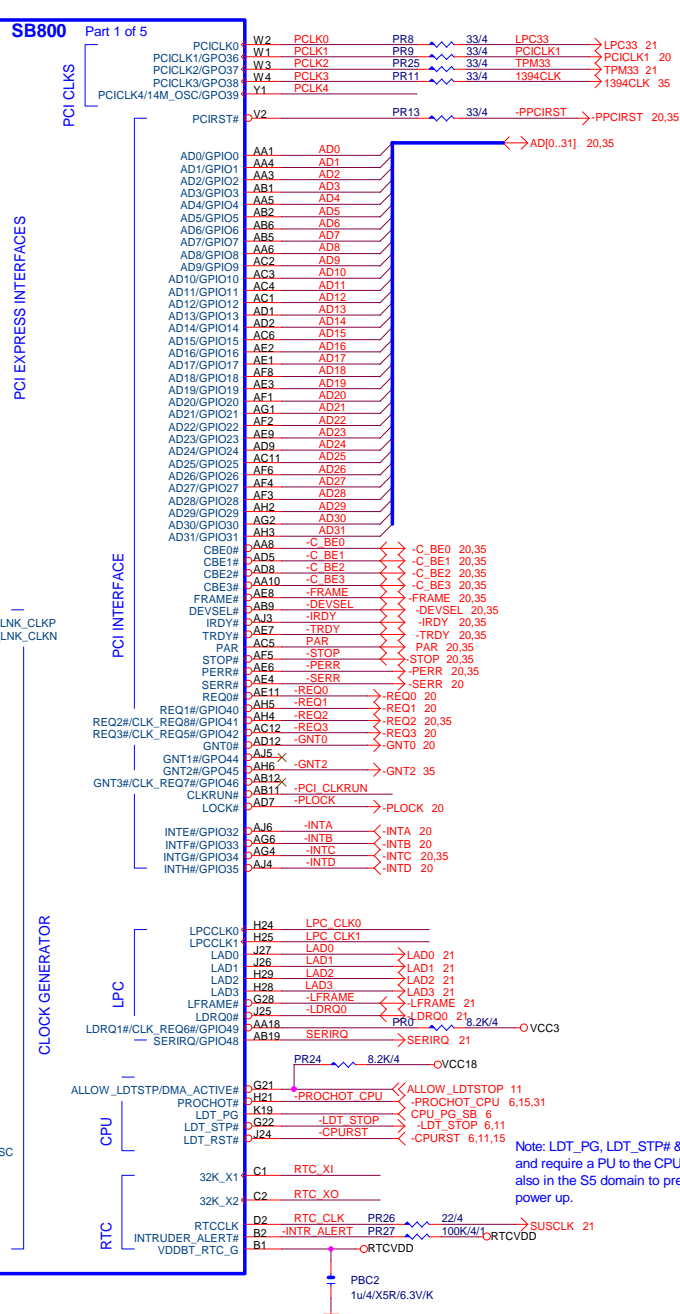
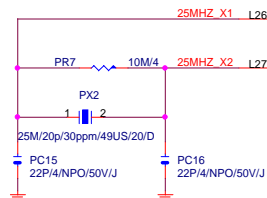
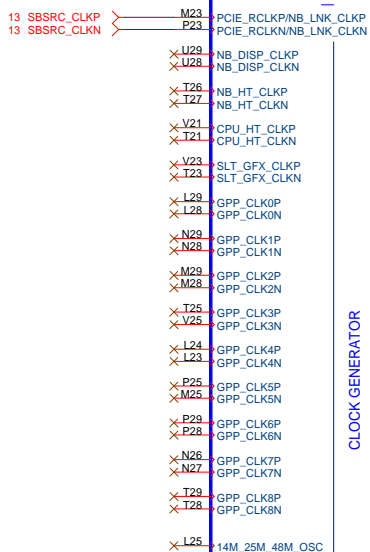
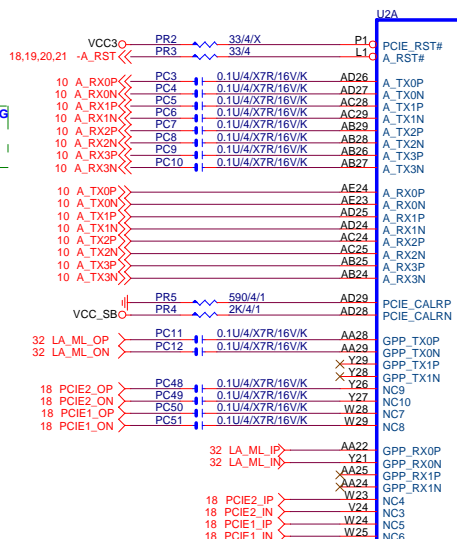
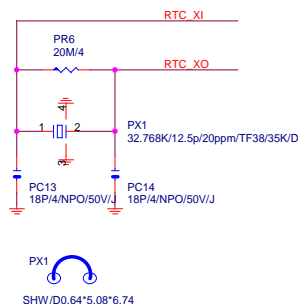
Document NumberGA-990FXA-UD3

Rev4.01

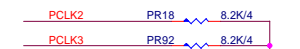
Date: Wednesday, July 17, 2013Sheet13 of 35



The diagram shows a square loop with two nodes labeled SB\_HS and SN. SB\_HS is at the top-left corner, and SN is at the bottom-right corner. The loop is formed by four blue lines. Red arrows point from the text labels to their respective nodes.

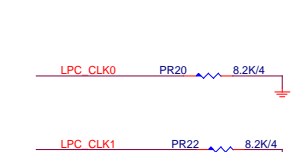


Low: Force PCIe GEN1, Up: Allow PCIe GEN2

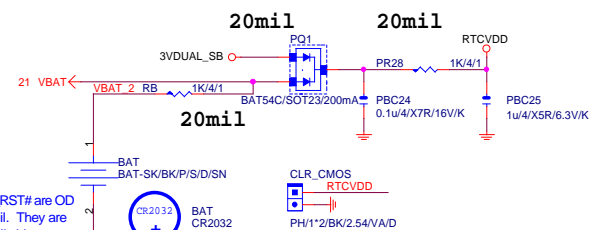


	PCLK2	PCLK3
<b>PULL HIGH</b>	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
<b>PULL LOW</b>	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting  
EC AOD-ACC



	LPC_CLK0 Rev.AT2	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	IMC DISABLED AOD Extreme DEFAULT	CLKGEN DISABLED DEFAULT



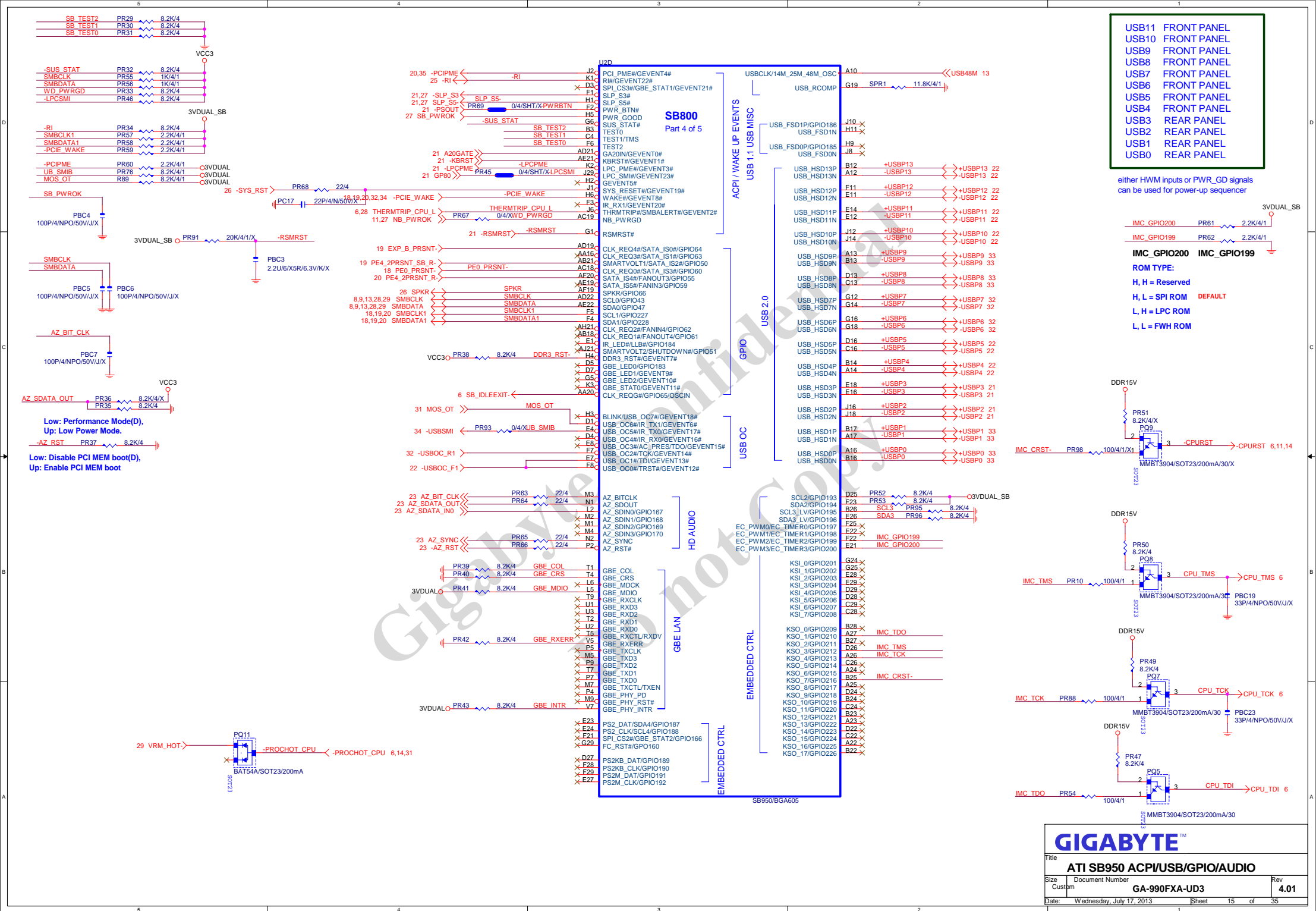
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

GIGABYTE™

Title	ATI SB950 PCIE/PCI/CPU/LPC
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Size Custom	Document Number <b>GA-990FXA-UD3</b>	Rev <b>4.01</b>
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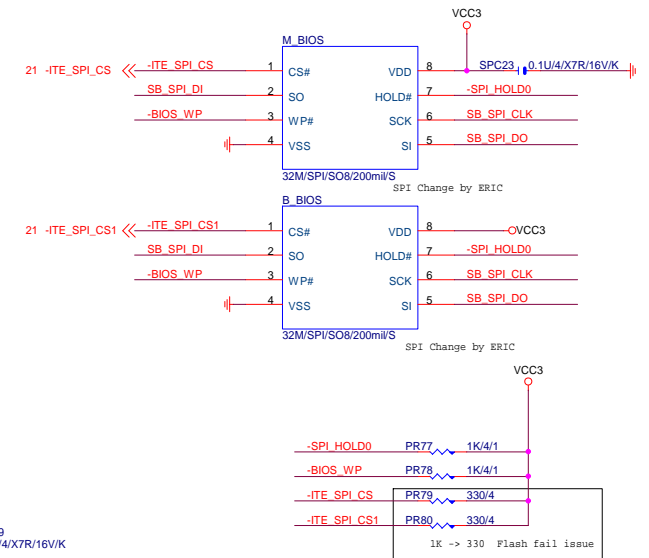
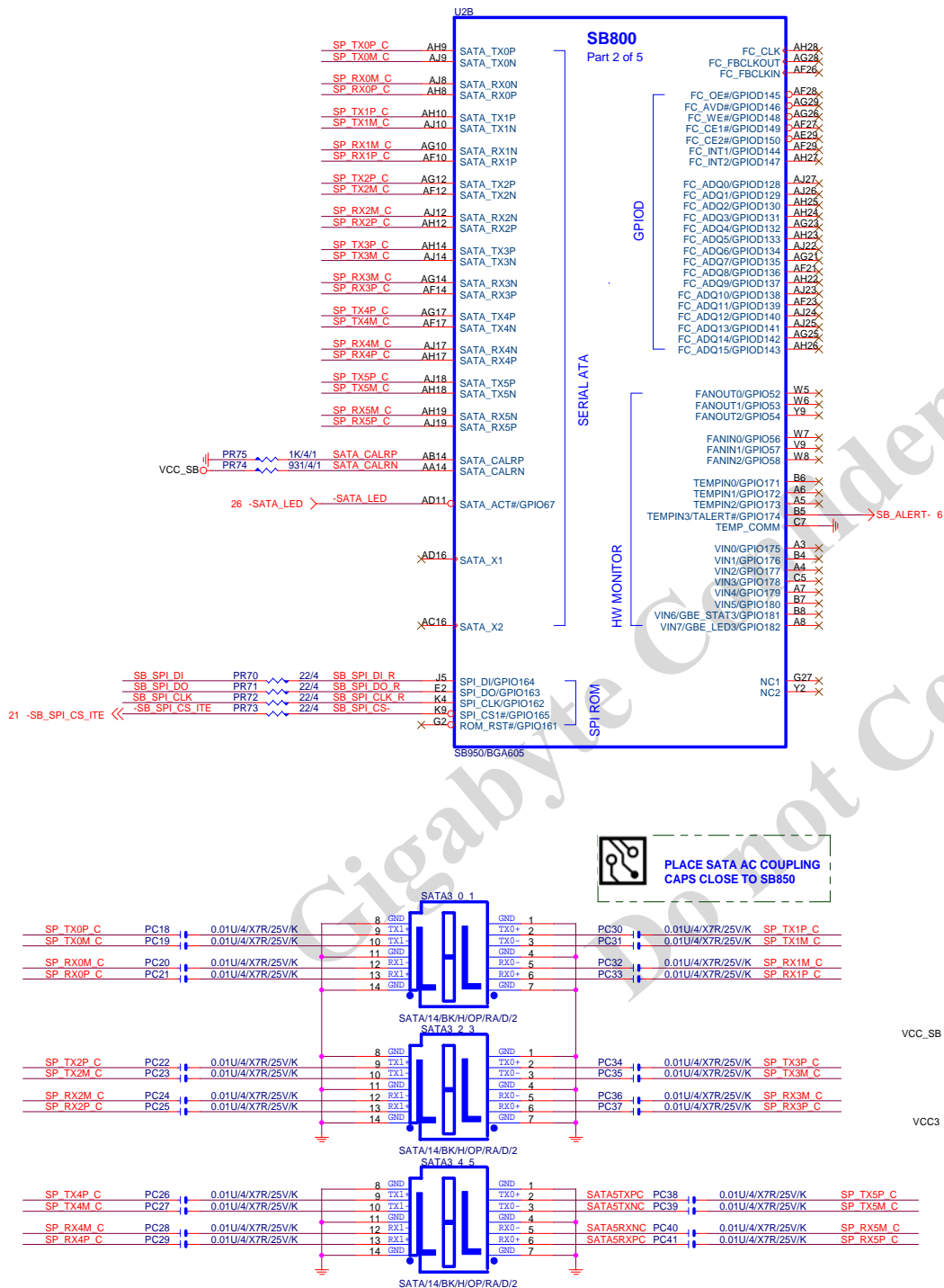
PLACE SATA CAL  
RES VERY CLOSE  
TO BALL OF U600

**NOTE:**

R650 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK



PLACE SATA AC COUPLING  
CAPS CLOSE TO SB850

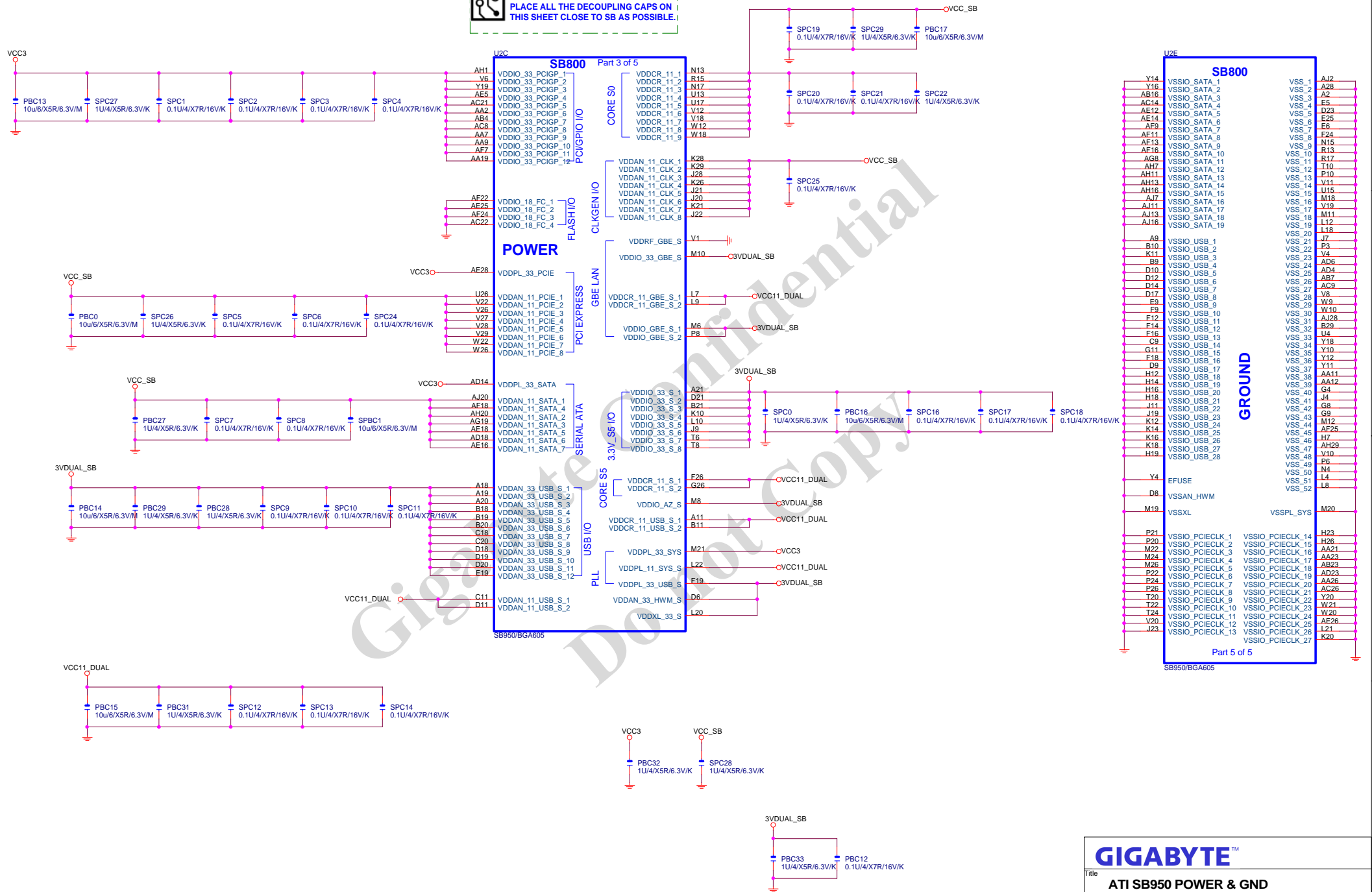


**GIGABYTE**

Title			ATI SB950 SATA/IDE/HWM/SPI
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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



**GIGABYTE**™

Title  
**ATI SB950 POWER & GND**

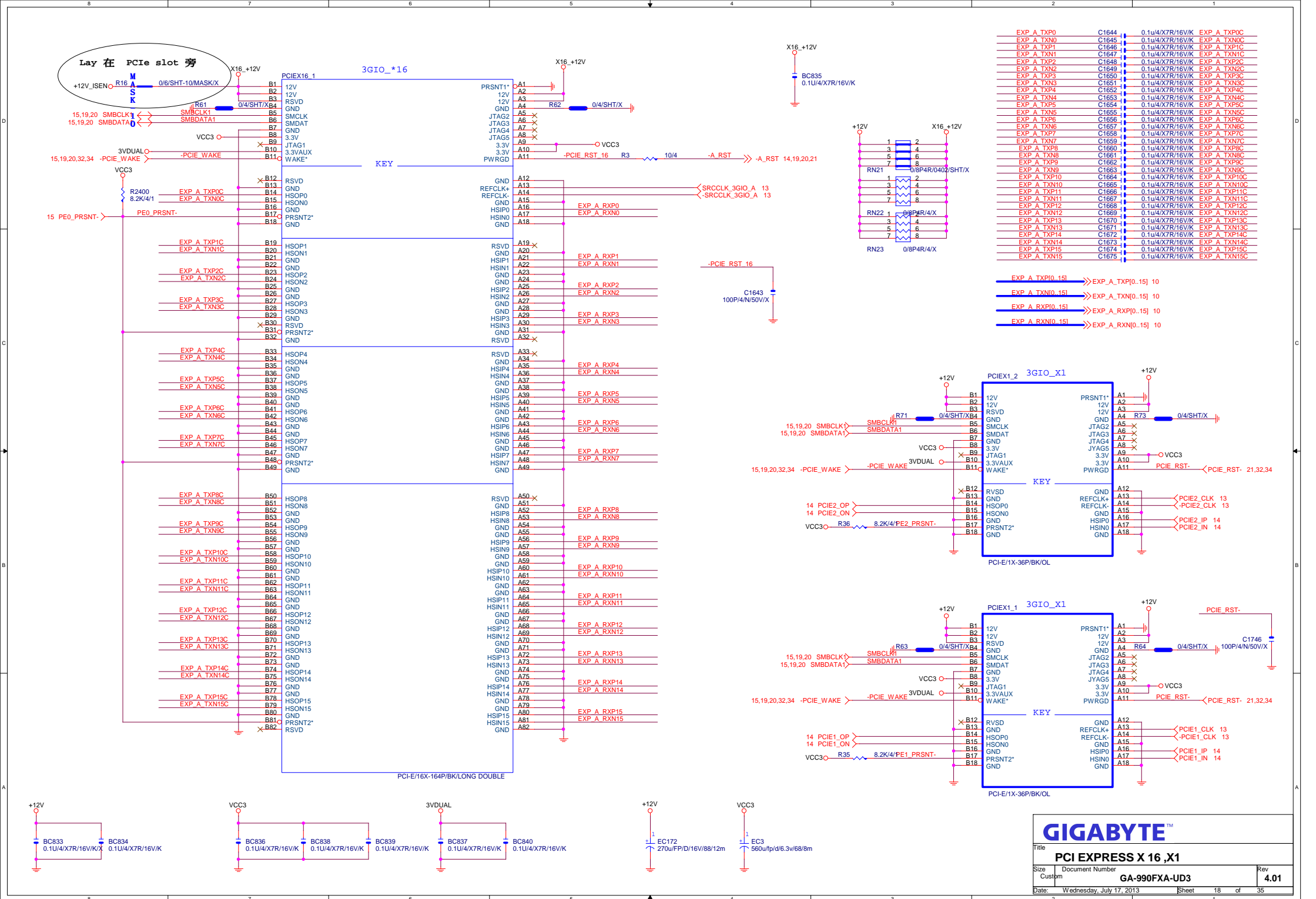
Size  
Custom

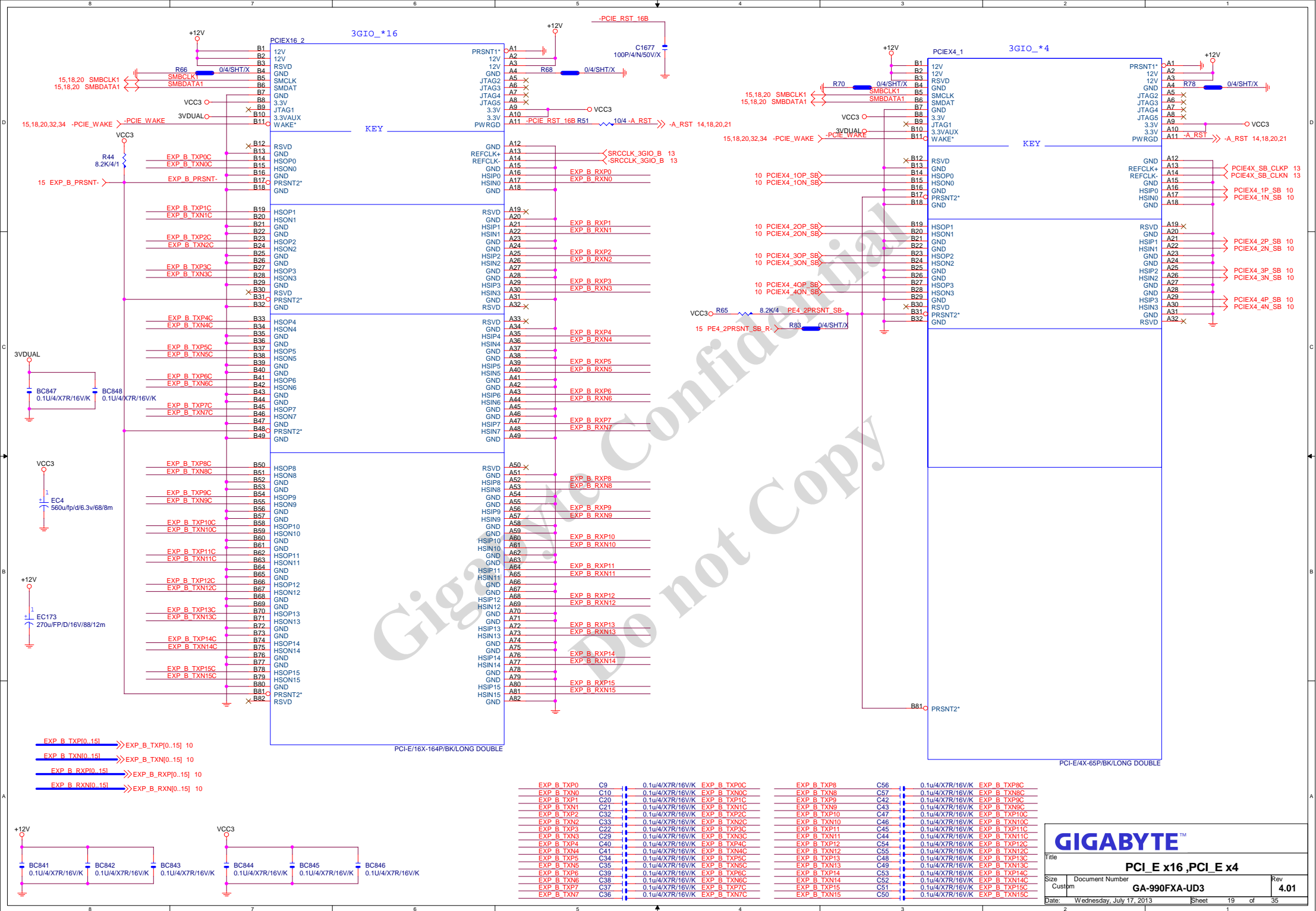
Document Number  
**GA-990FXA-UD3**

Date: Wednesday, July 17, 2013

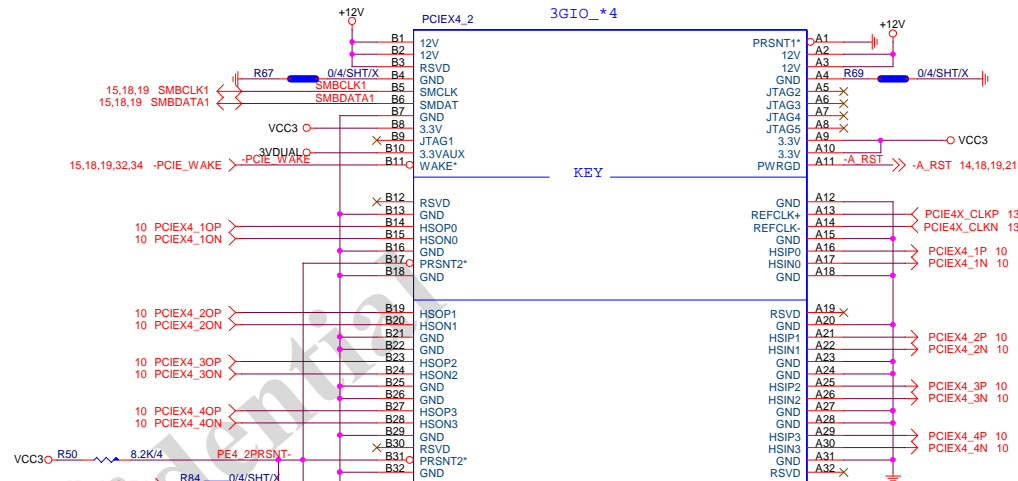
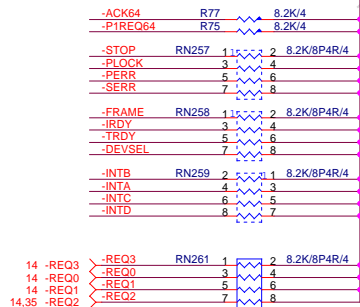
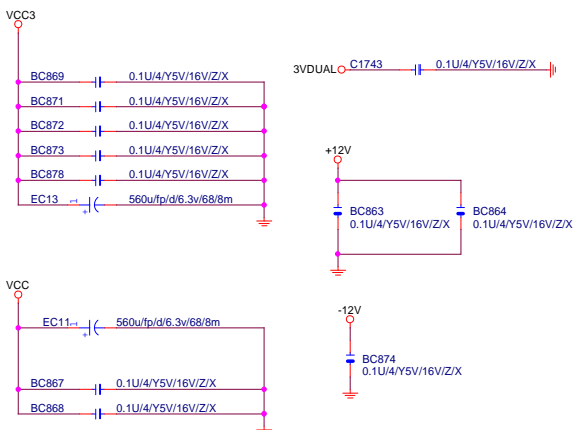
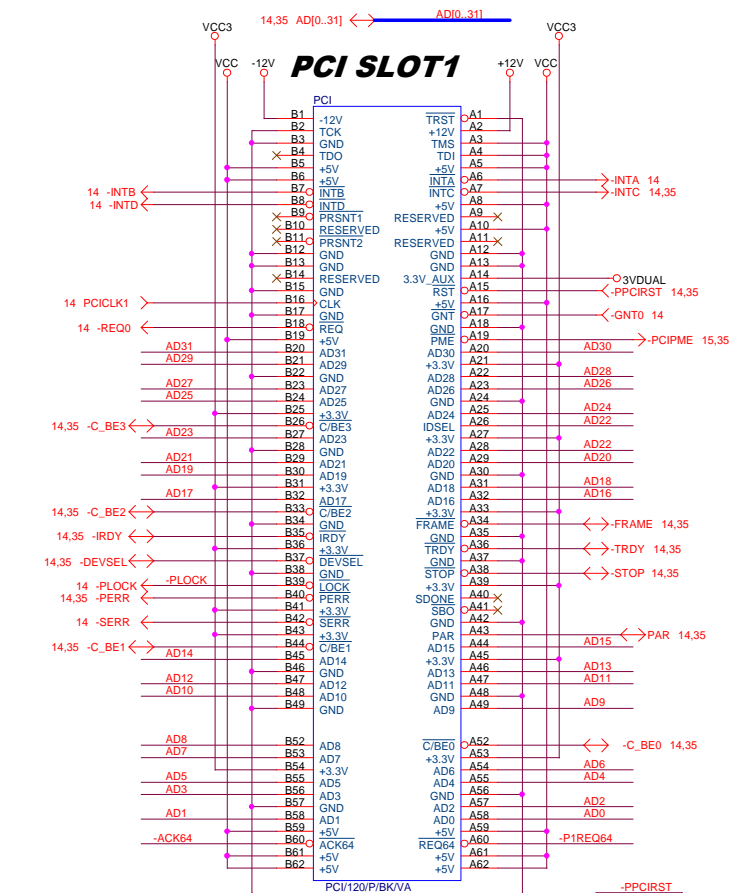
Sheet 17 of 35

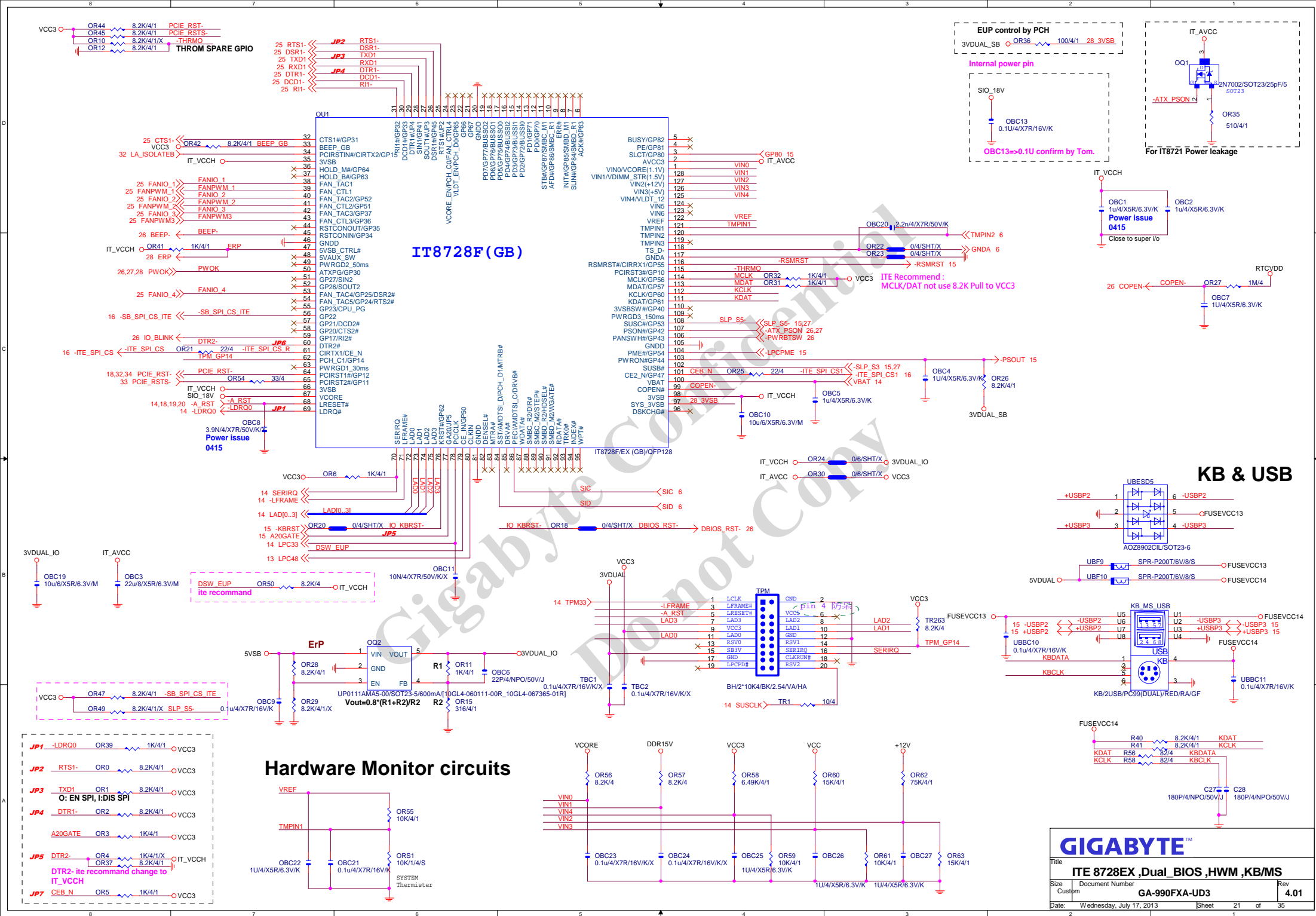
Rev  
**4.01**

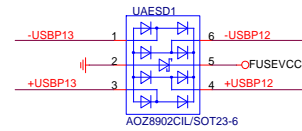
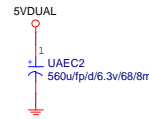
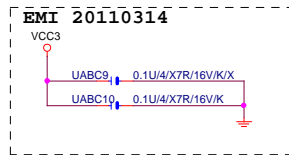




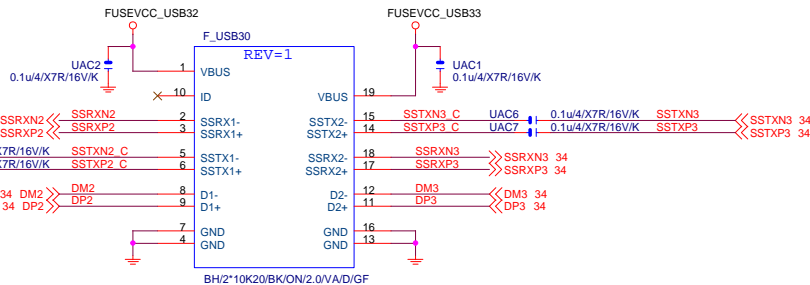
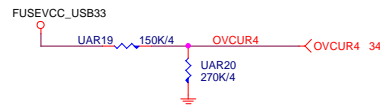
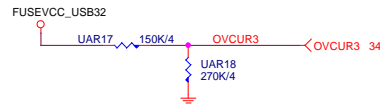
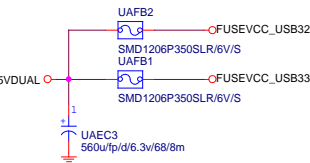
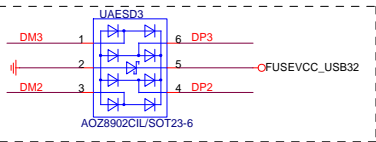
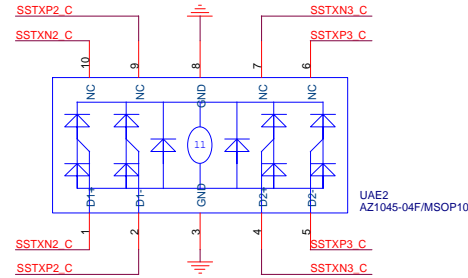
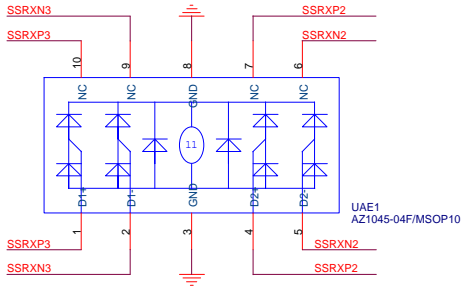
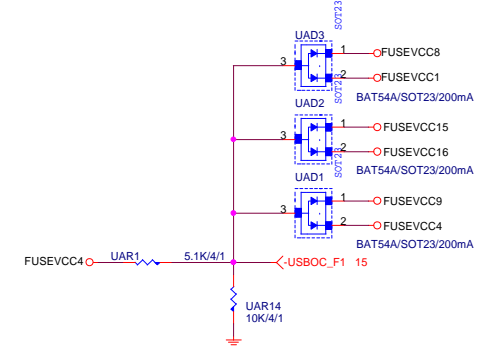
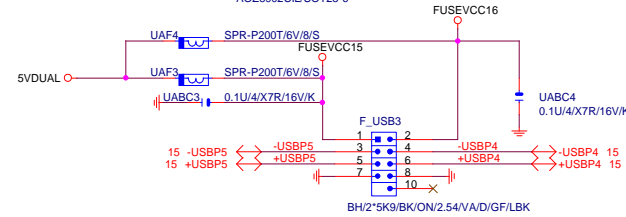
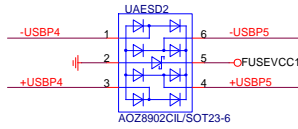
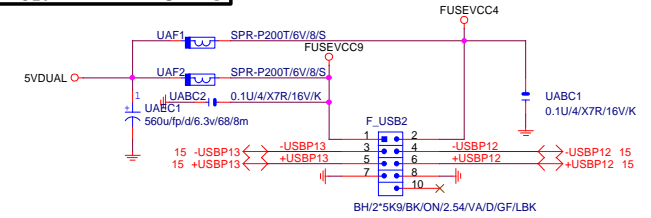
# PCI SLOT1



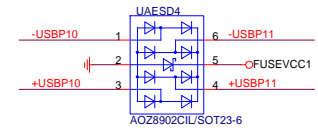
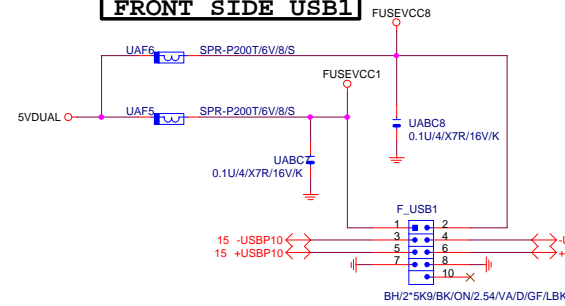




## FRONT SIDE USB3

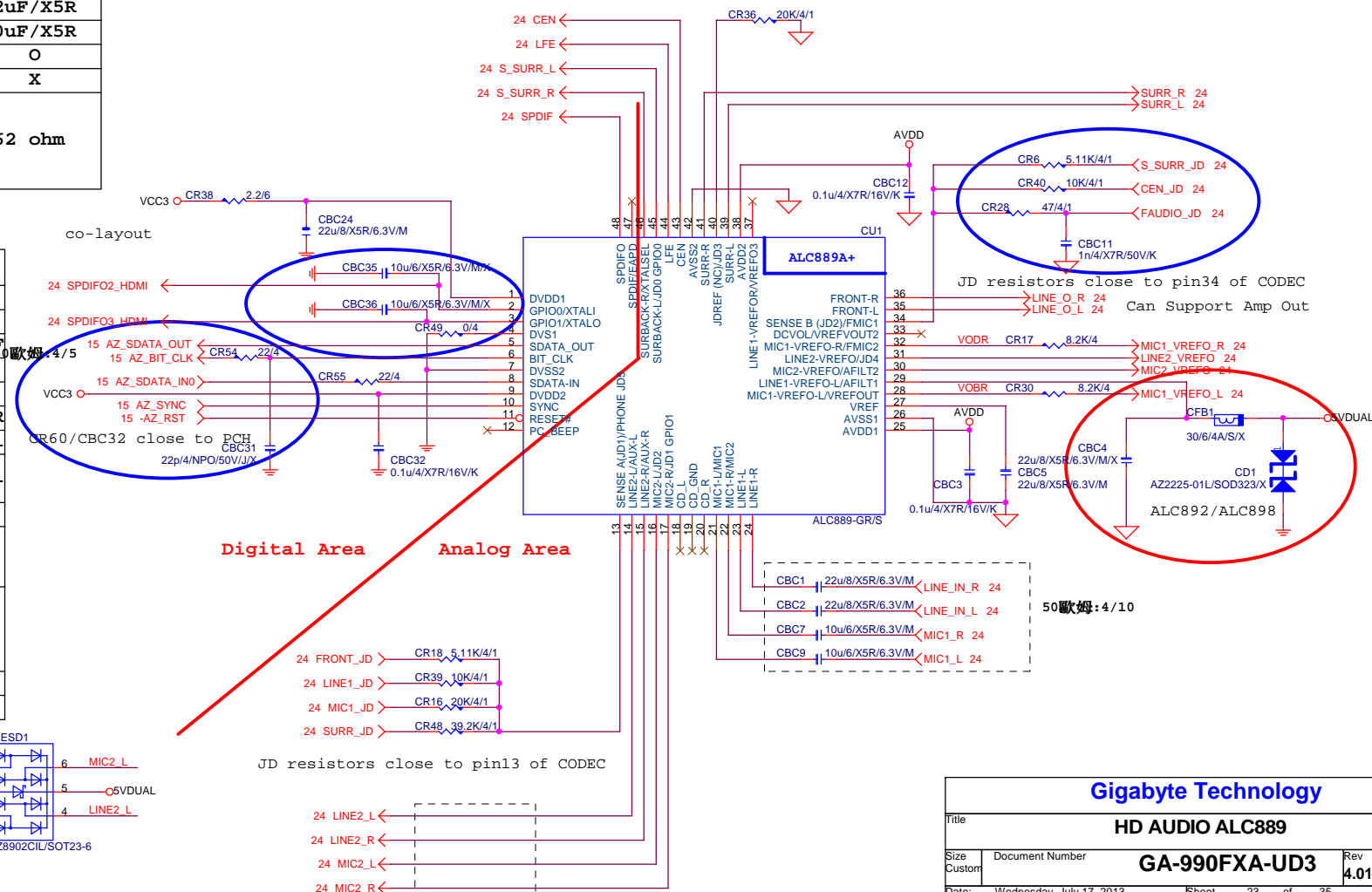


## FRONT SIDE USB1



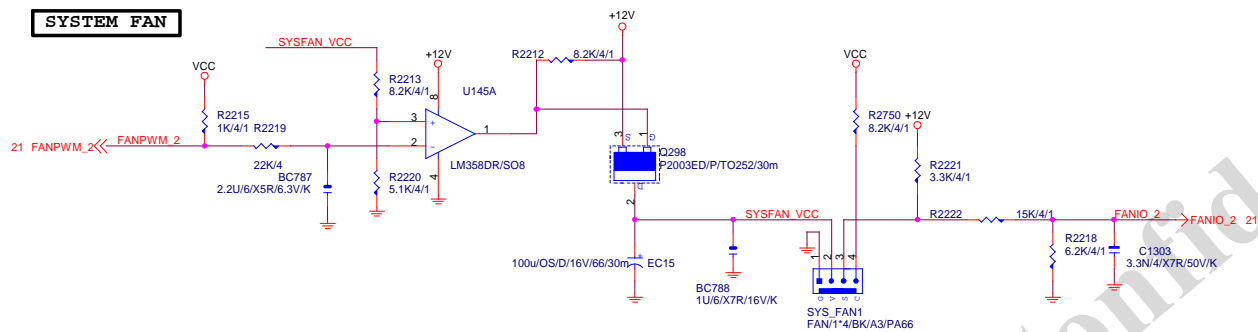
**GIGABYTE**

Title			COM/LPT/F_USB	
Size	Document Number	GA-990FXA-UD3		Rev
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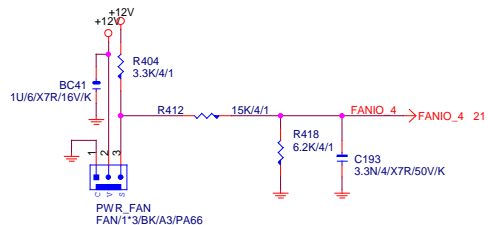
ALC889/VT2021 Colay



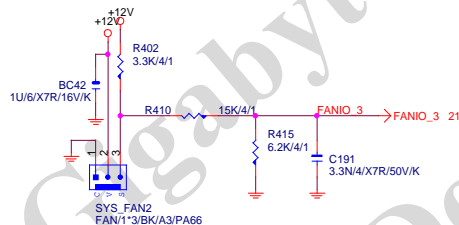
# SYSTEM FAN



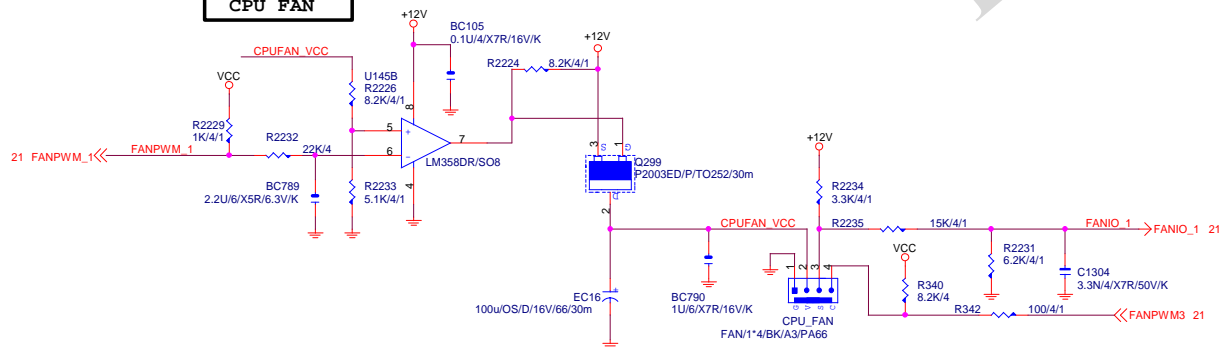
# POWER FAN



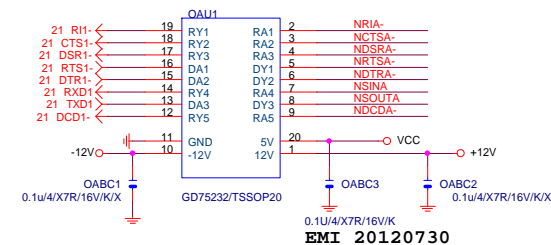
# SYSTEM FAN2



# CPU FAN

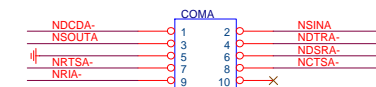
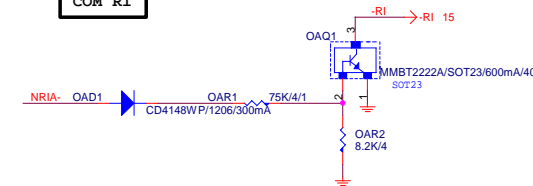


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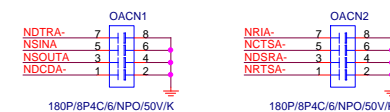
EMI 20120730

# COM RI



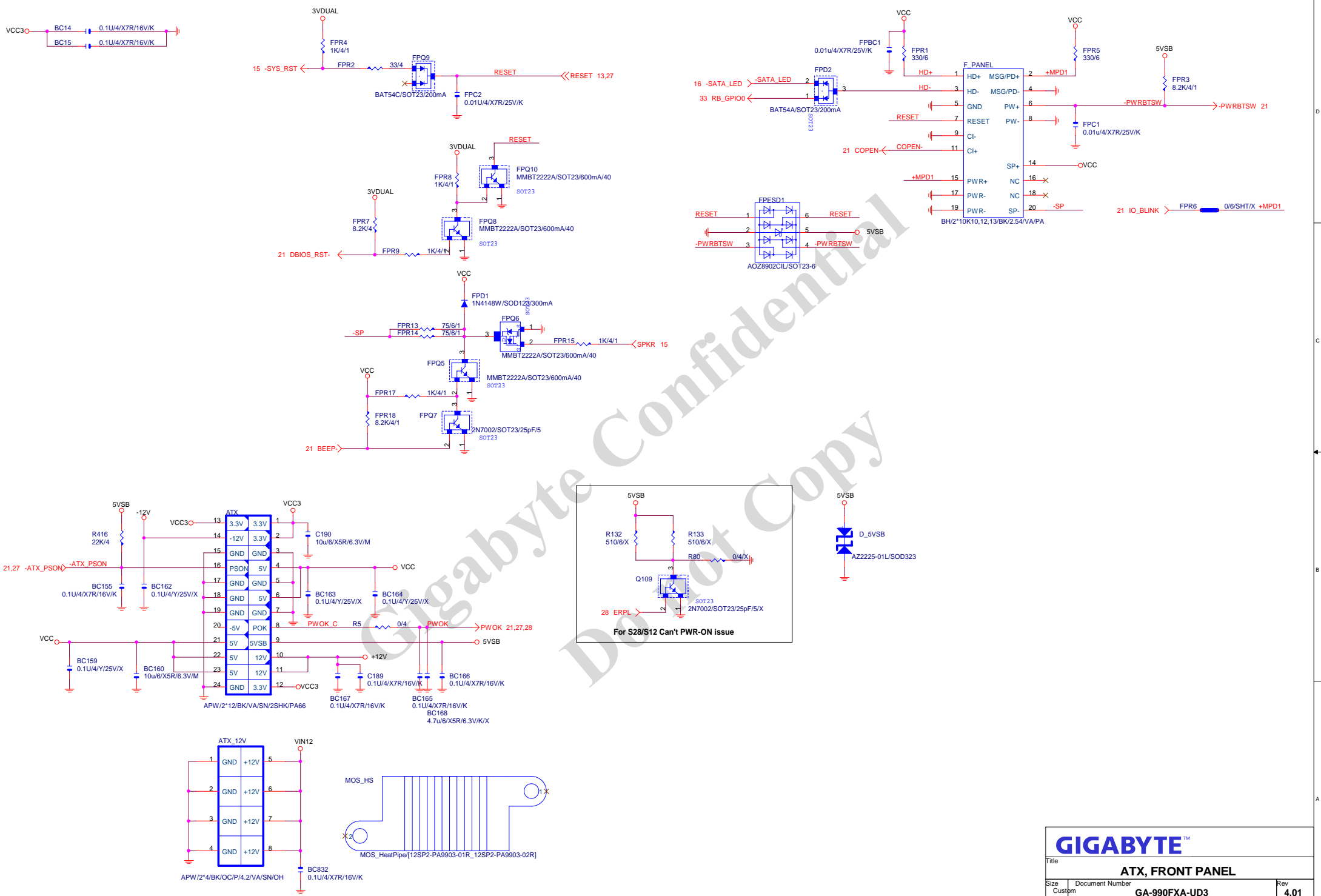
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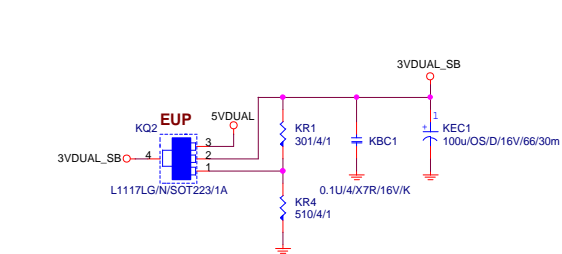
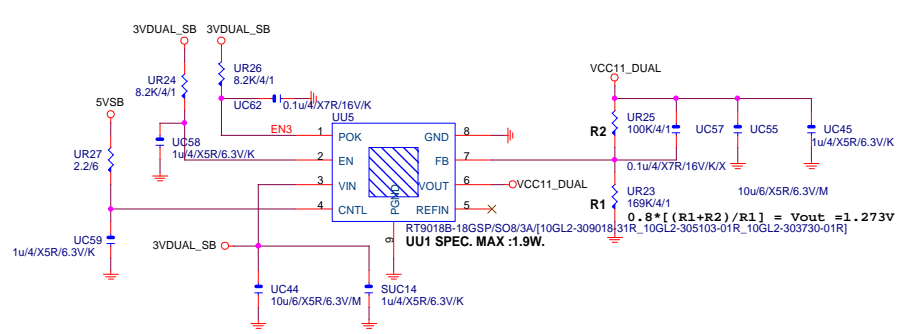
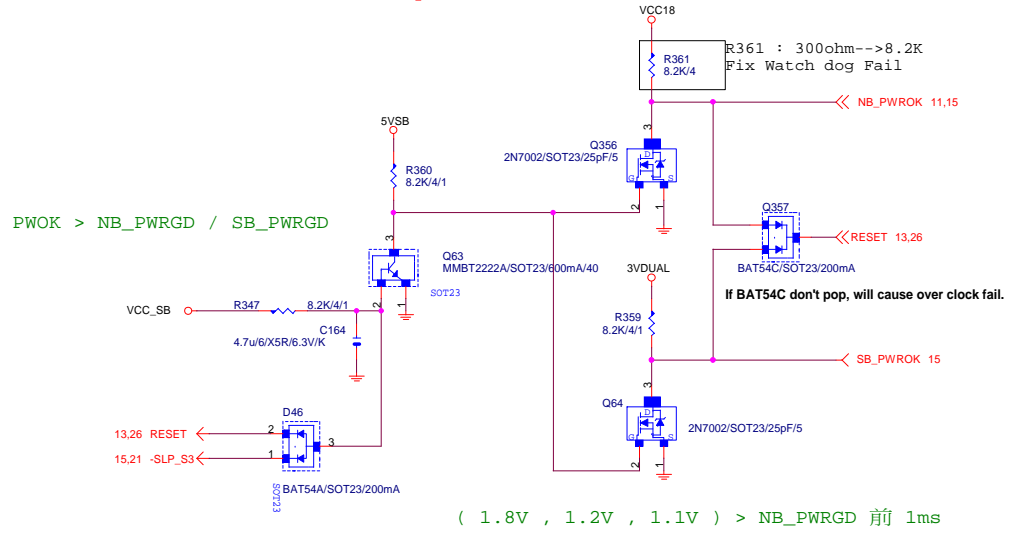
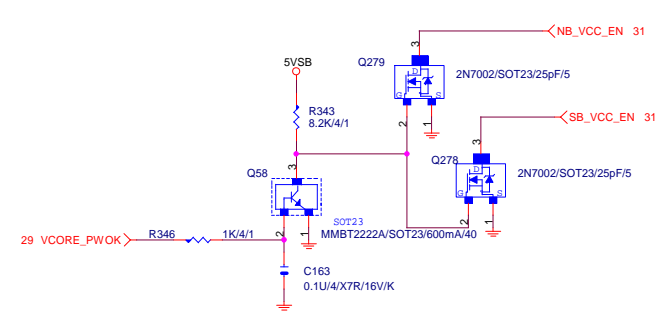
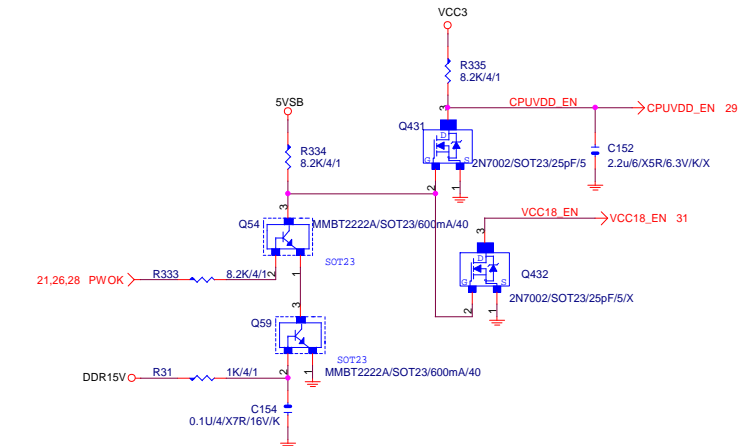
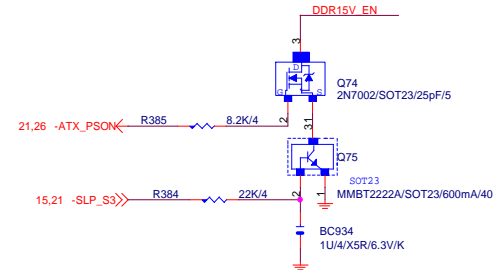
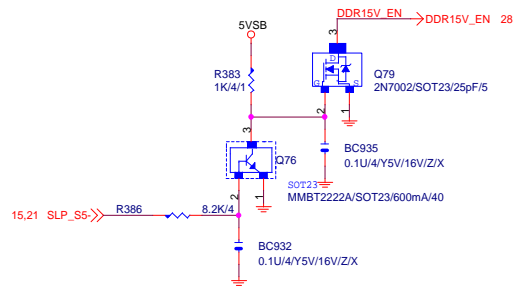
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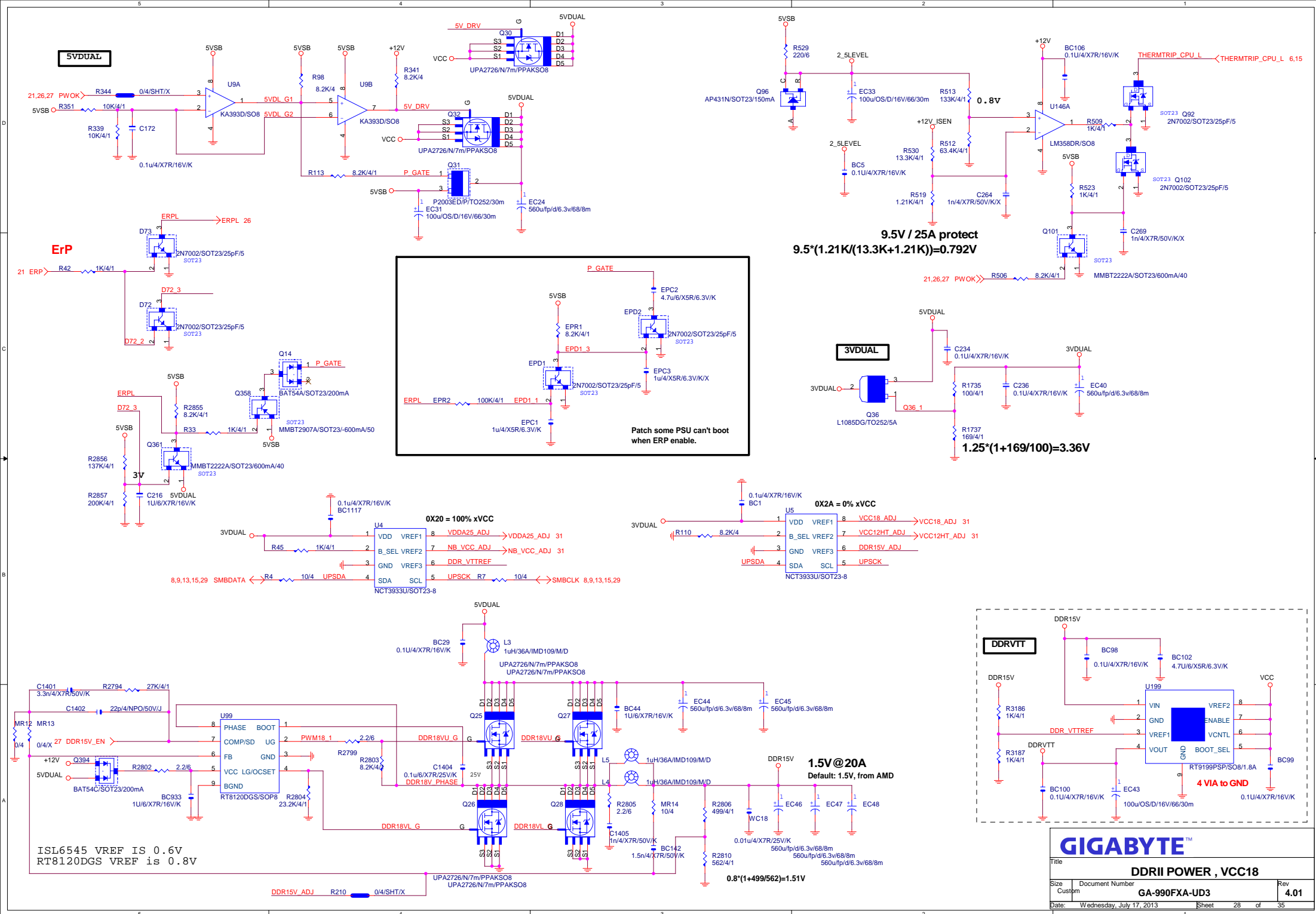


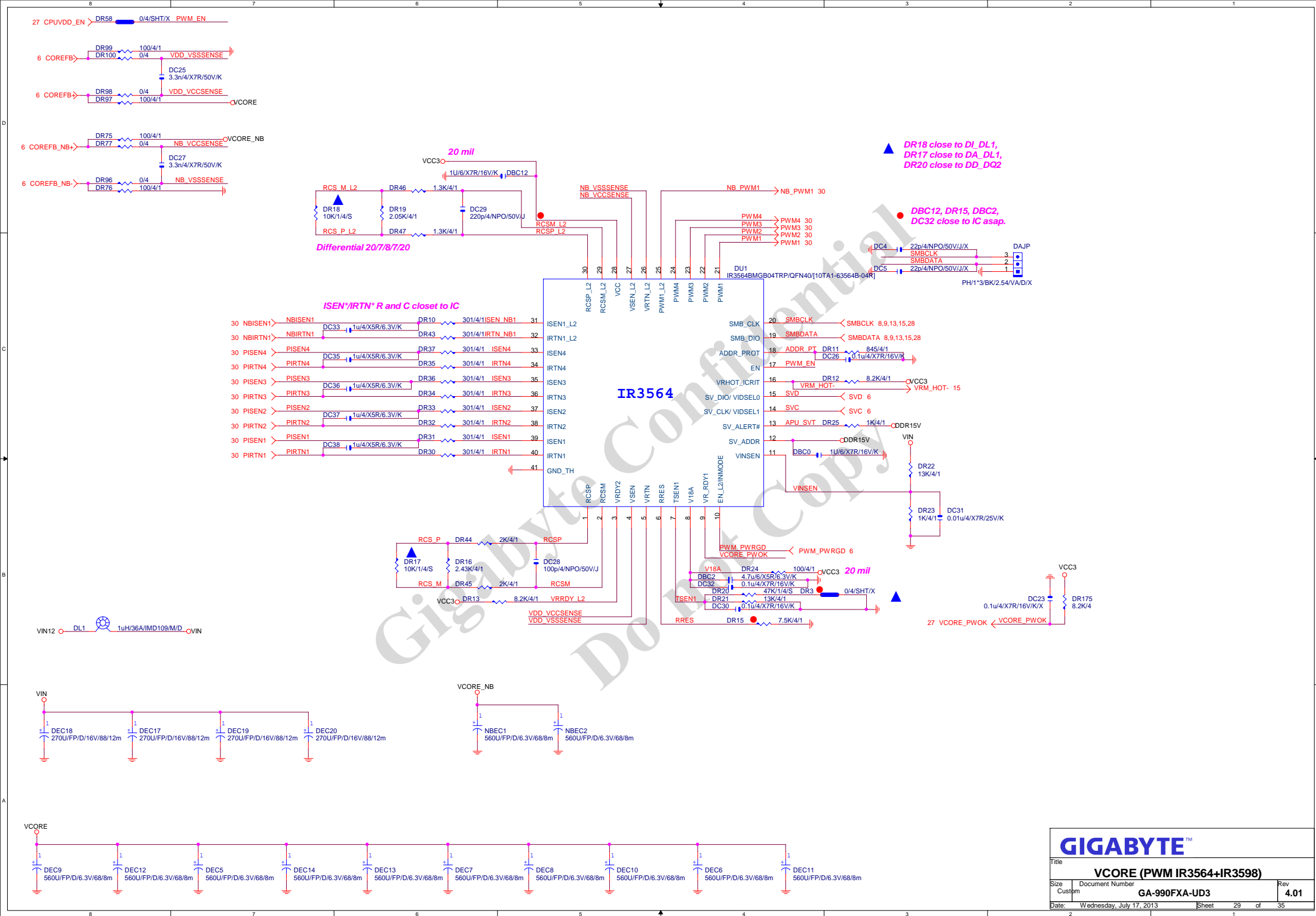
**GIGABYTE**

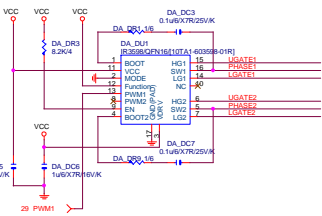
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Size	Document Number	GA-990FXA-UD3	
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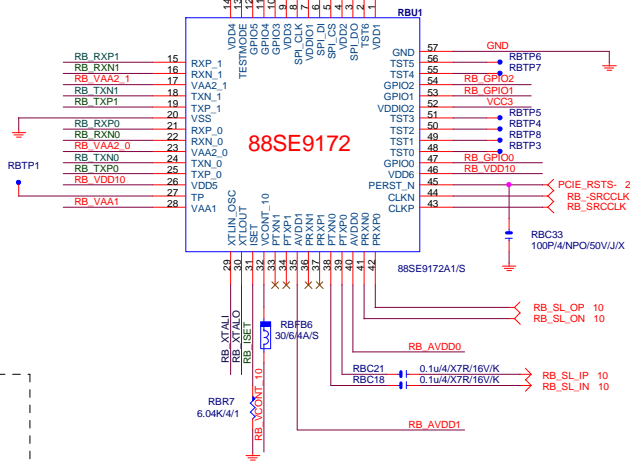
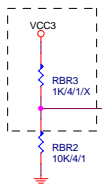
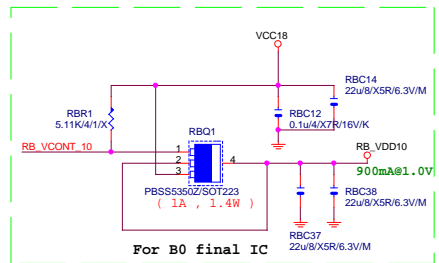
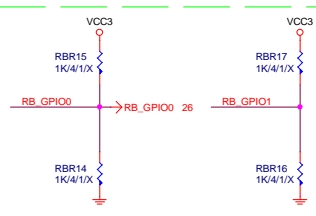
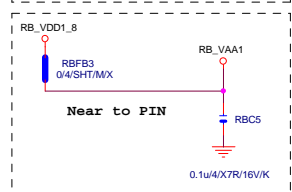
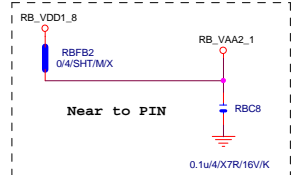
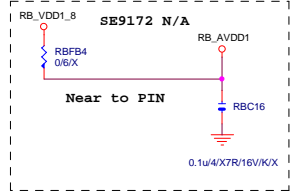
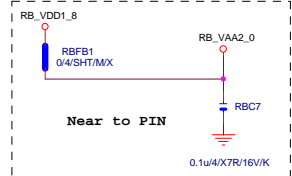
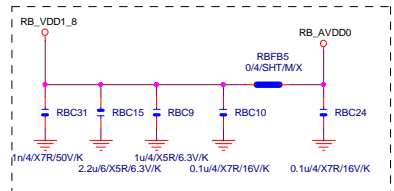
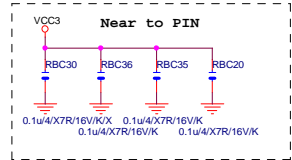
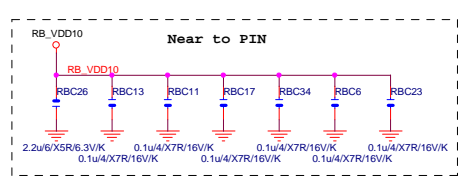




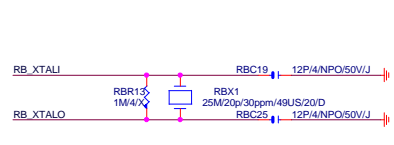
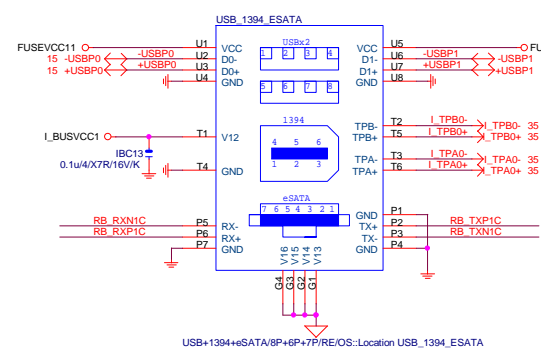
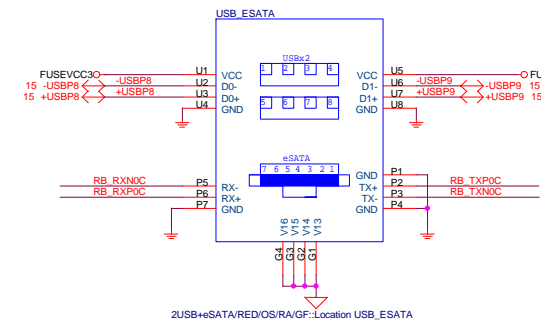
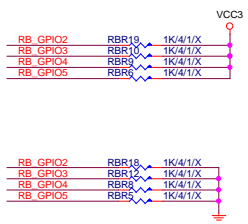
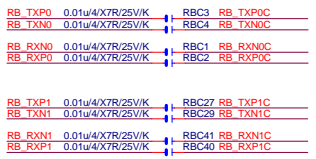
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7	7	24	24
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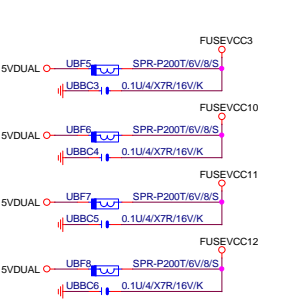
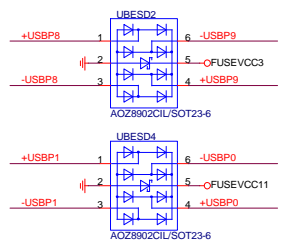
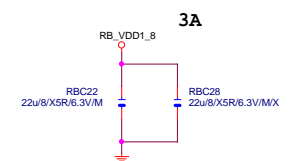
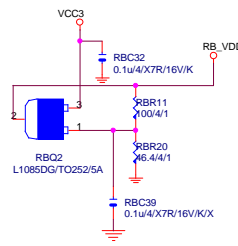




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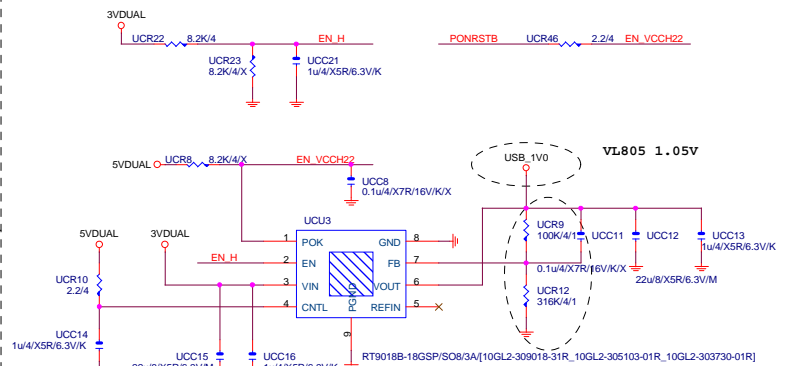
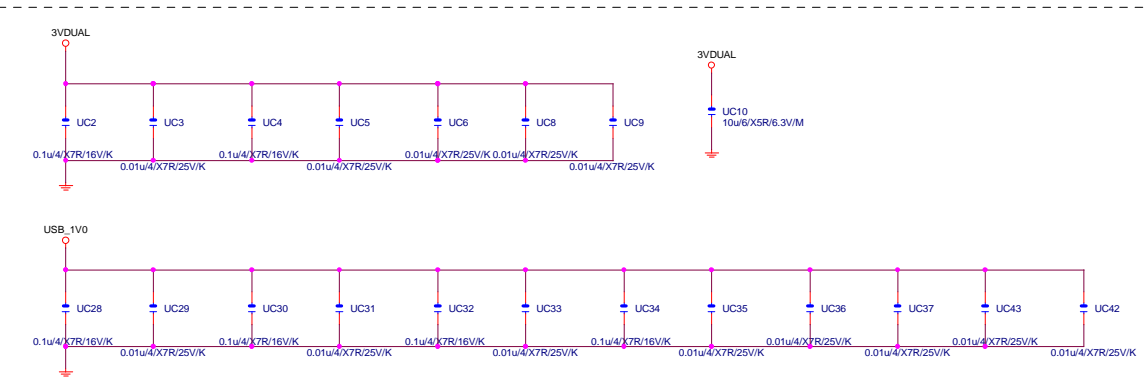
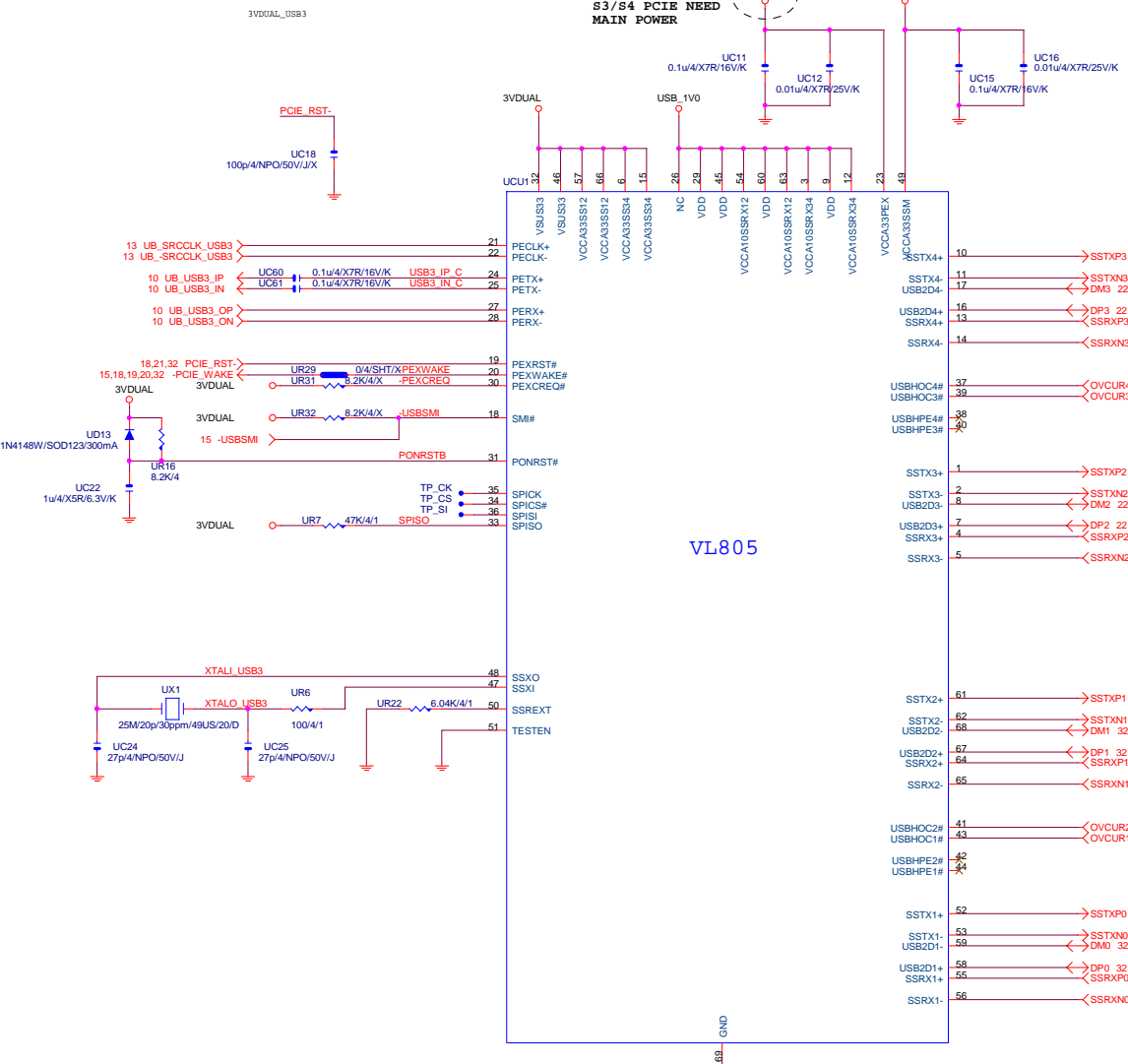


### 3.3V to 1.8V Voltage Regulator



Gigabyte Technology			
Marvell 9172_ESATA			
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【技術通報R&D技術通報156】  
RT9018 (RICHTEK) 與 NCT3730 (NUVOTON),  
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份  
須做修改為 100K 以上電阻值

